

COMPAL CONFIDENTIAL

MODEL NAME : QAM00
PCB NO : LA-7731P
BOM P/N : 4319ET31L01
GPIO MAP:

Dalmore 12 UMA


Ivy Bridge + Panther POINT
2011-8-30
REV : 0.3 (X01)
@ : Nopop Component
CONN@ : Connector Component

MB Type	BOM P/N	
M/B SPI ROM		5@
TAA SPI ROM		6@
SATA re-driver with CD function		7@
Normal E-SATA re-driver		8@

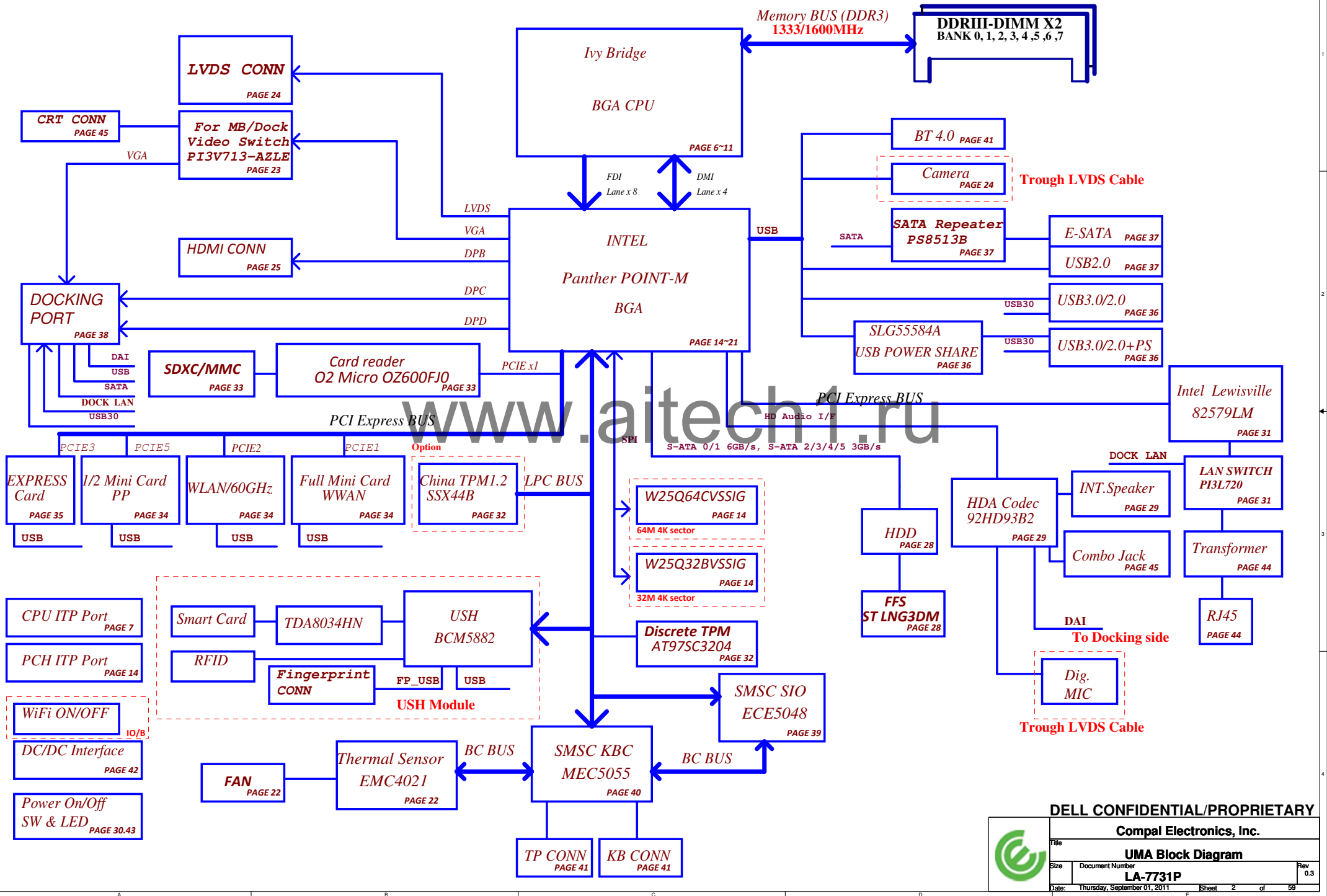
MB PCB	
Part Number	Description
DA60000P700	PCB OFH LA-7731P REV0 M/B UMA

@HDMI Royalty	
Part Number	Description
RO0000002HM	HDMI Royalty

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Block Diagram



POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M (M-OFF)	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and PM Table

SATA	DESTINATION
SATA 0	HDD
SATA 1	NA
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Right side)
	1	JUSB2 (Bot side)
	2	NA
	3	MLK DOCK
	4	WLAN
	5	WWAN
	6	JMINI3(PP)
	7	USH->BIO
	8	DOCKING
	9	JESATA1 (Left)
	10	Express card
	11	Bluetooth
	12	Camera
	13	NA
USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	None
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

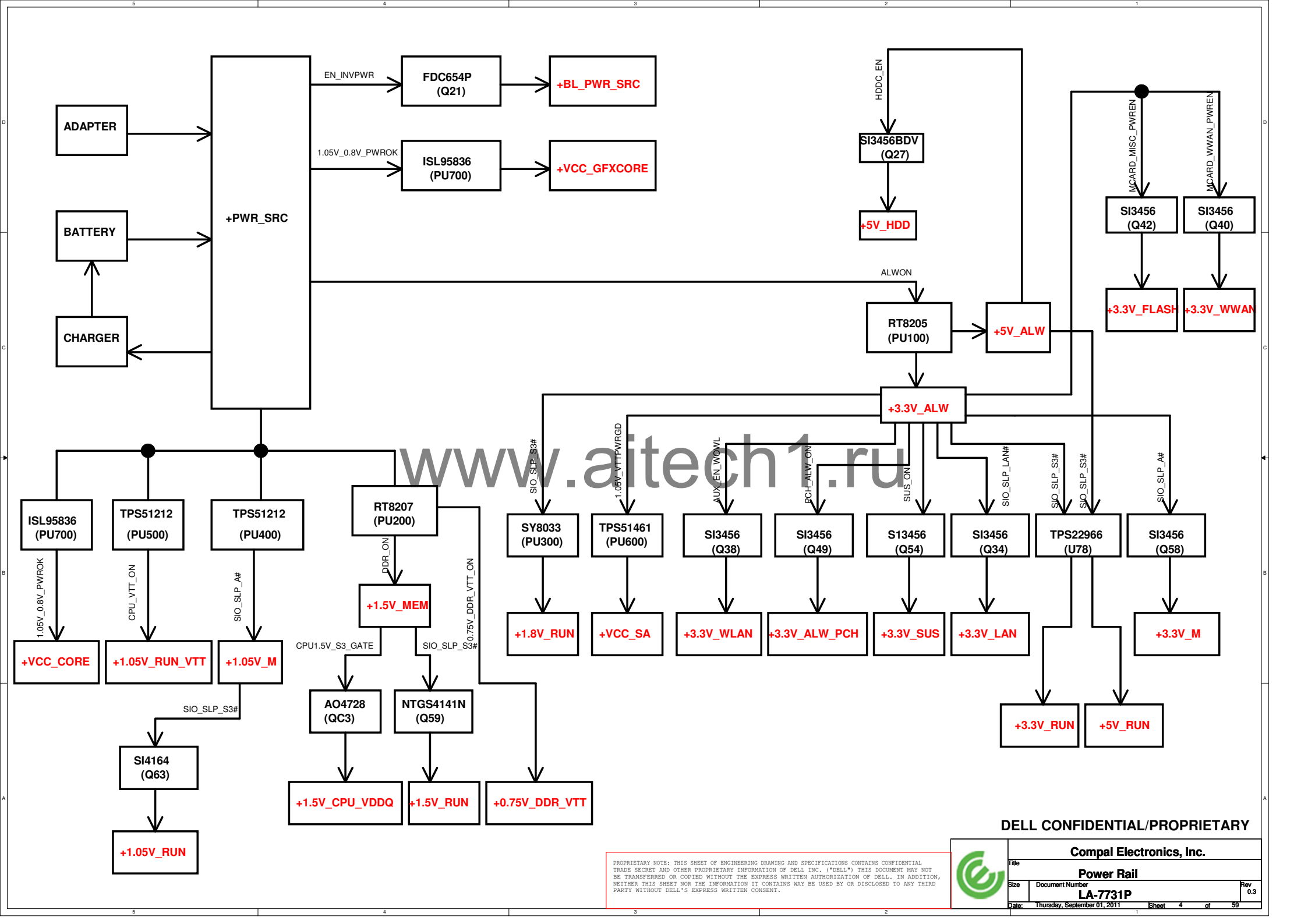
UMA DP/HDMI Port	Connetion
Port B	MB HDMI Conn
Port C	Dock DP port 2
Port D	Dock DP port 1

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50
			Add Plating		1.00
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080	2.60
2	GND/PWR		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
3	Slg 1		Copper foil	1oz	1.35
		4.7	Prepreg	7628HRC+2116HRCx2+7628HRC	23.60
4	Slg 2		Copper foil	1oz	1.35
		3.7	Core	4mil	3.91
5	GND/PWR		Copper foil	1oz	1.35
		3.7	Prepreg	1080	2.60
6	Bottom		Copper foil	0.5oz	0.65
			Add Plating		1.00
			SolderMask		0.50
Overall Thickness (1.2mm ± 10%)				47.6	46.32000

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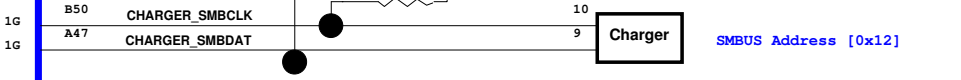
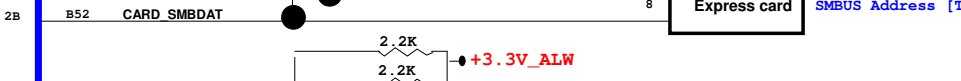
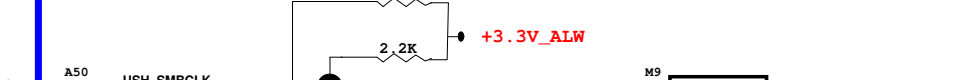
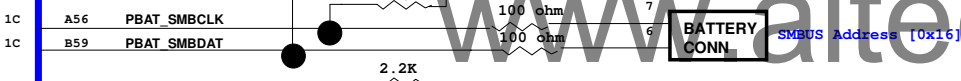
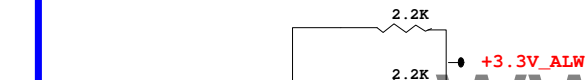
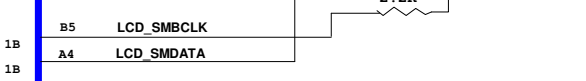
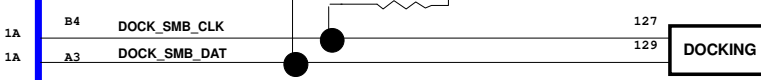
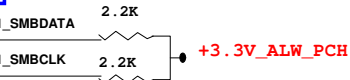
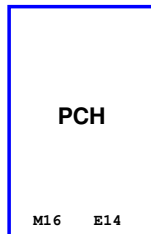
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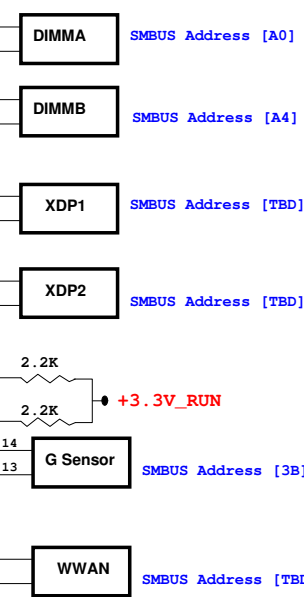
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Power Rail			
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SMBUS Address [0x9a]



SMBUS Address
APR_EC: 0x48
SPR_EC: 0x70
MSLICE_EC: 0x72
USB: 0x59
AUDIO: 0x34
SLICE_BATTERY: 0x17
SLICE_CHARGER: 0x13



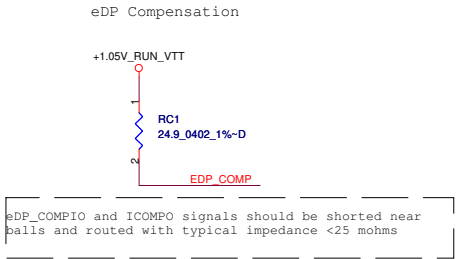
MEC 5065

KBC

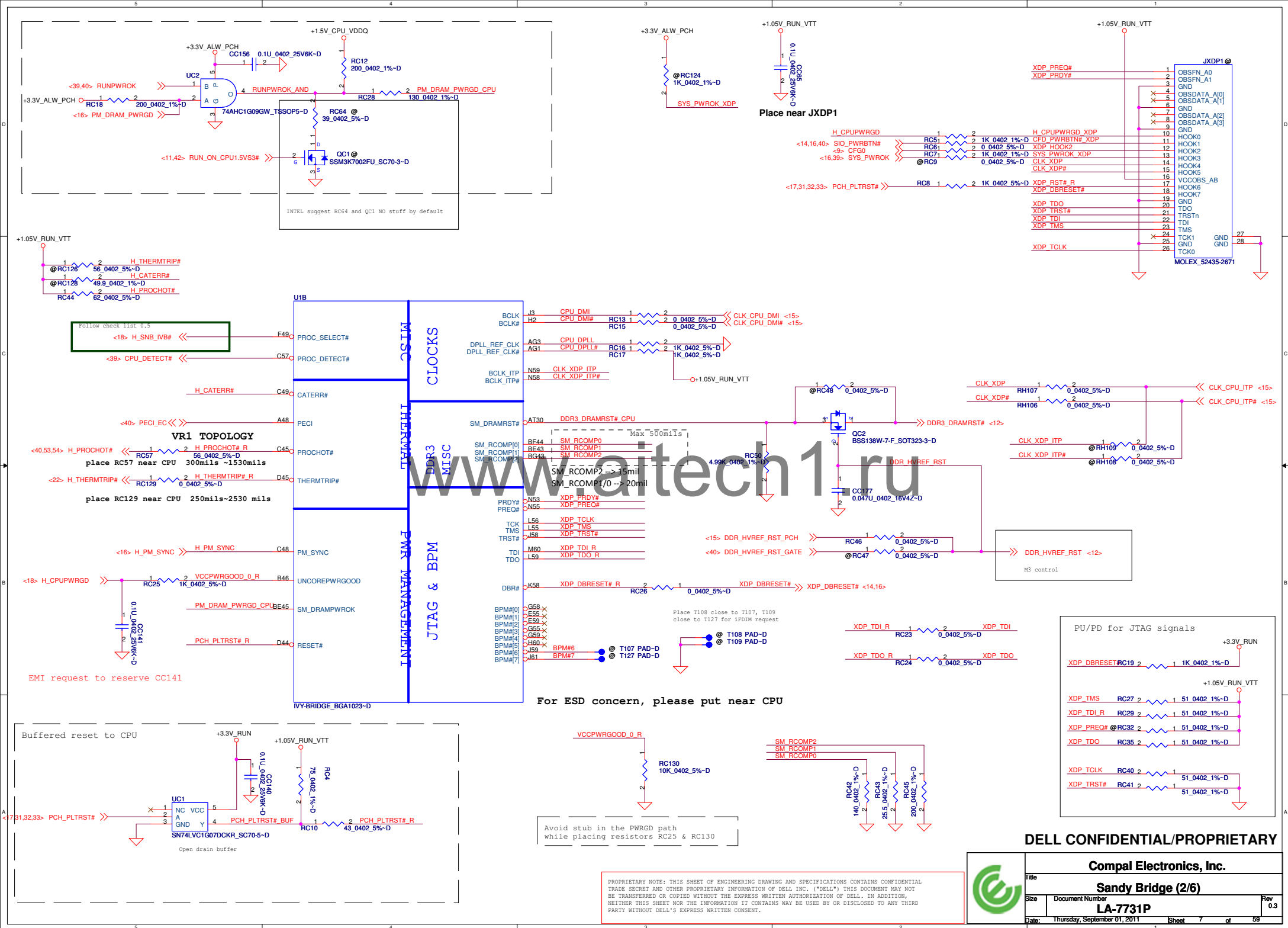
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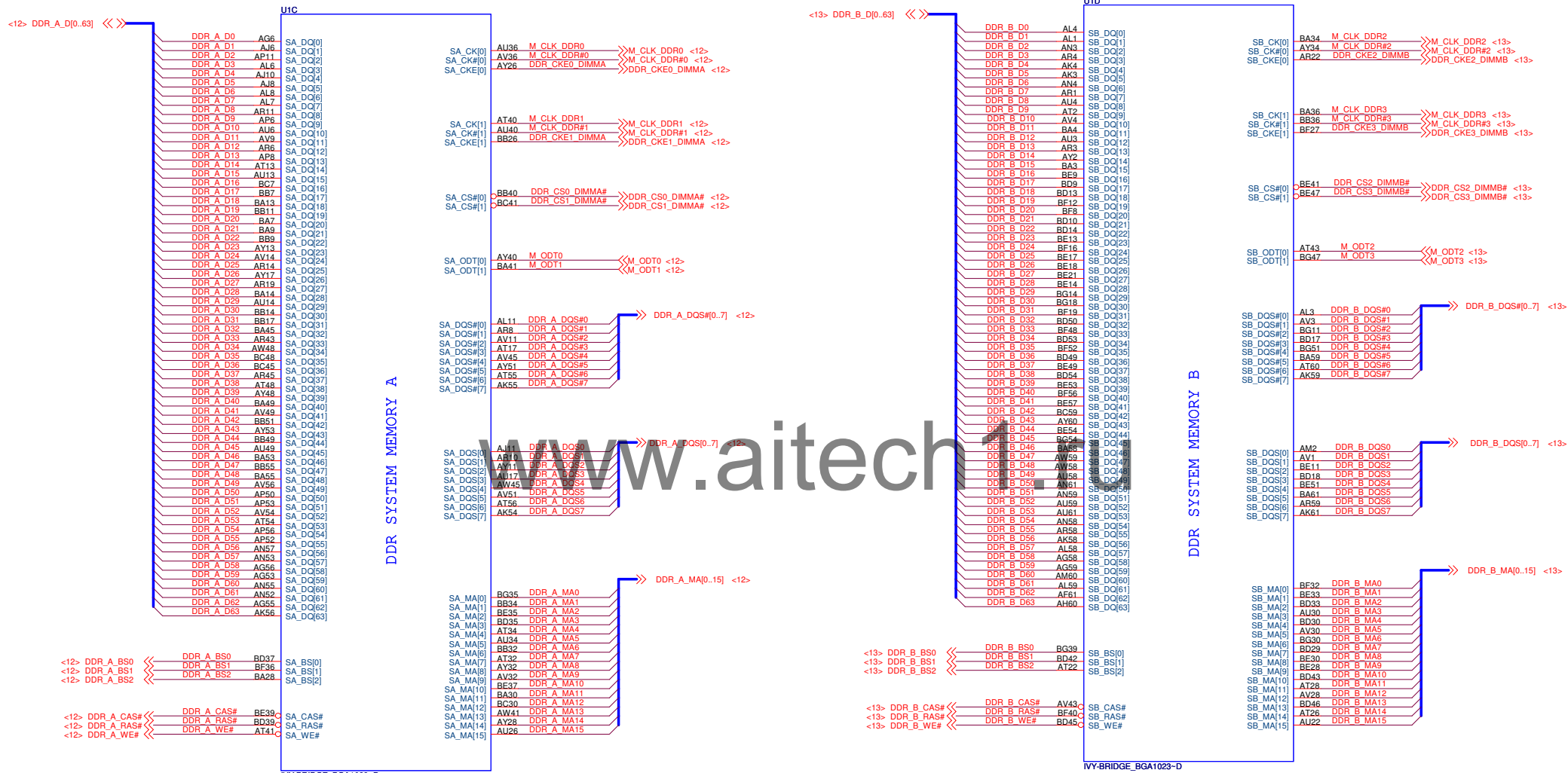
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms

PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



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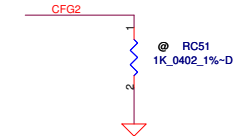
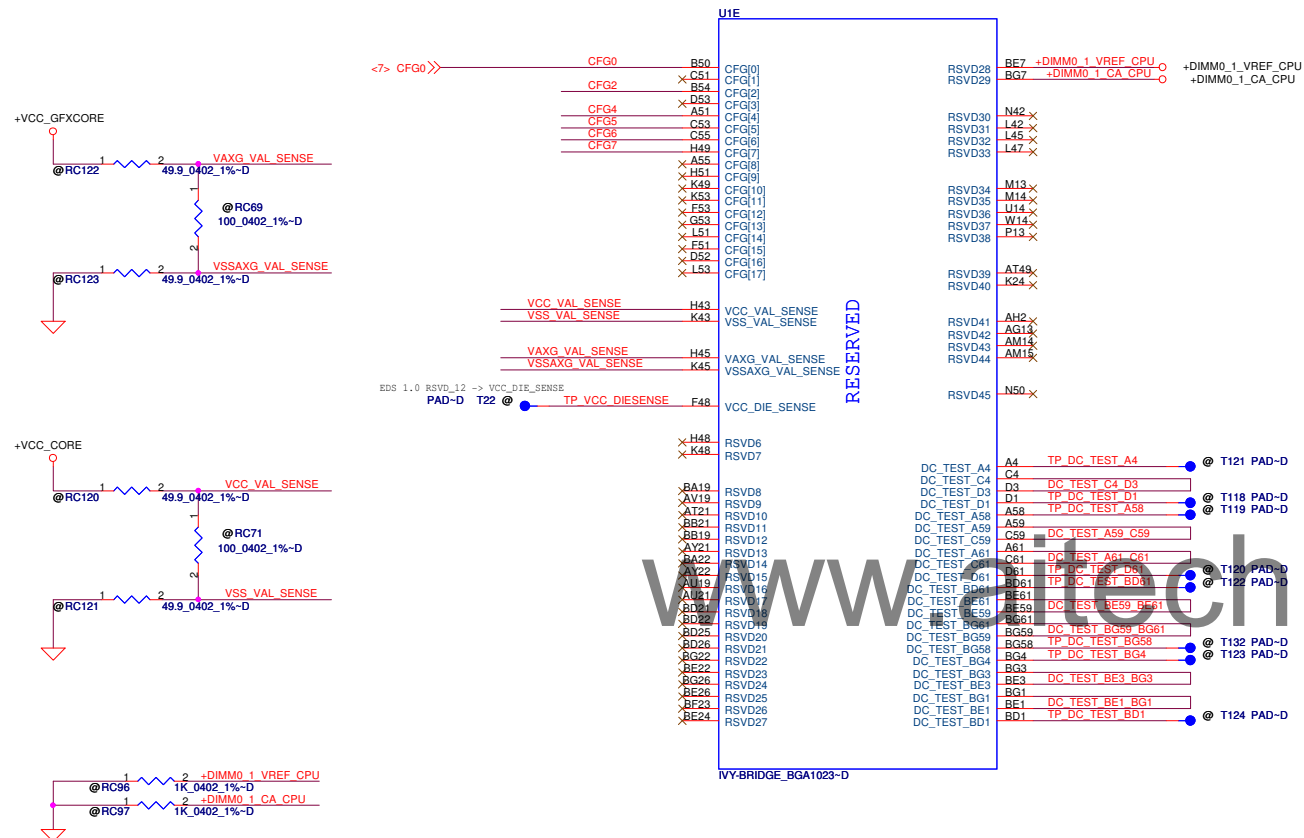


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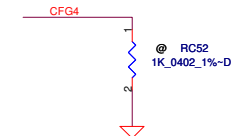
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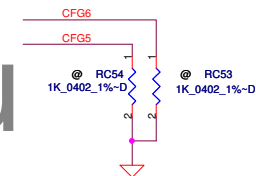
CFG Straps for Processor



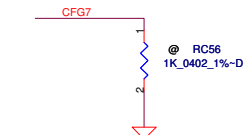
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

H=4mm
+V_DDR_REFA_M3 RD7 2 0.0402 5%-D
+V_DDR_REF RD1 2 0.0402 5%-D
+DIMM1_VREF_DQ
+1.5V_MEM
+1.5V_MEM 2-3A to 1 DIMMs/channel

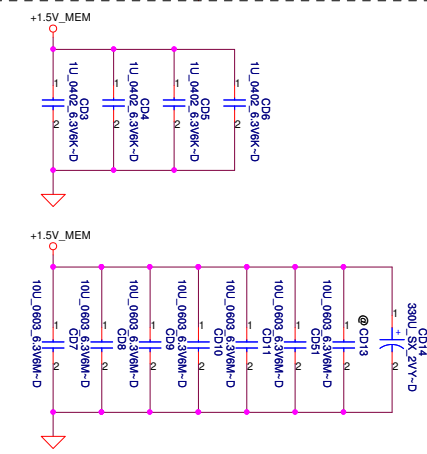
Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

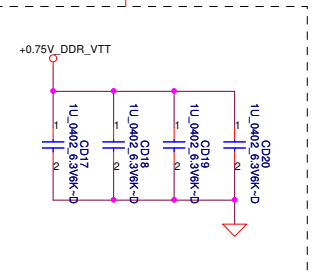
<8> DDR_A_DQS#0..7 <<>>
<8> DDR_A_D0..D3 <<>>
<8> DDR_A_DQS#0..7 <<>>
<8> DDR_A_MA0..15 <<>>

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

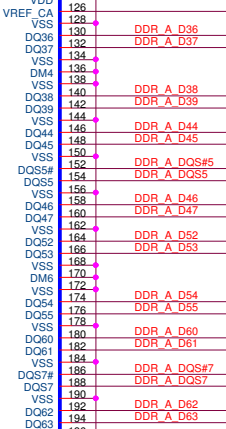
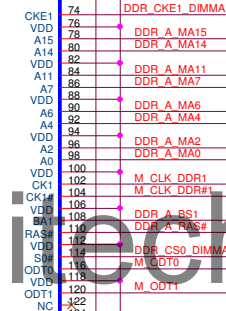
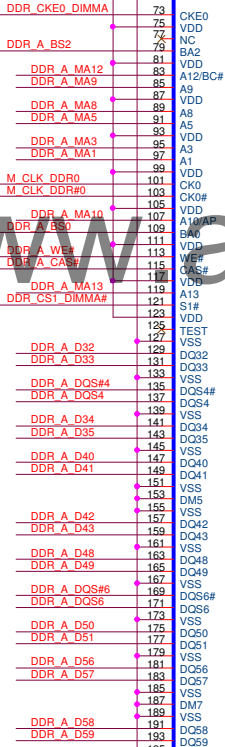


Layout Note:
Place near JDIMM1.203,204

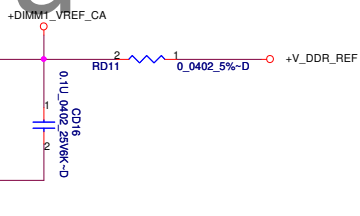
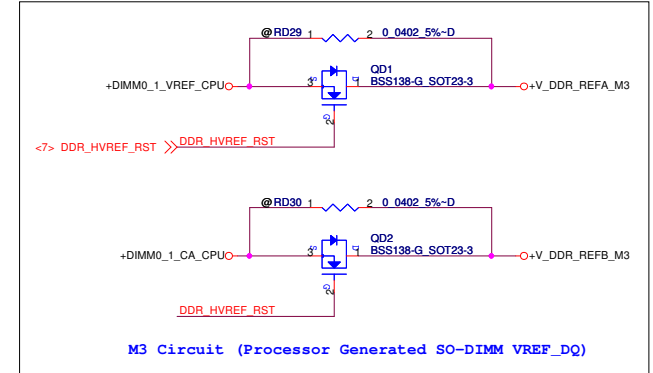


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<8> DDR_A_BS2 <<>>

<8> M_CLK_DDR0 <<>>
<8> M_CLK_DDR#0 <<>>
<8> DDR_A_BS0 <<>>
<8> DDR_A_WEX <<>>
<8> DDR_A_CAS# <<>>
<8> DDR_CS1_DIMMA# <<>>



<13> DDR3_DRAMRST#_R <<>> RD28 2 1K 0402 1%-D <<>> DDR3_DRAMRST# <7>

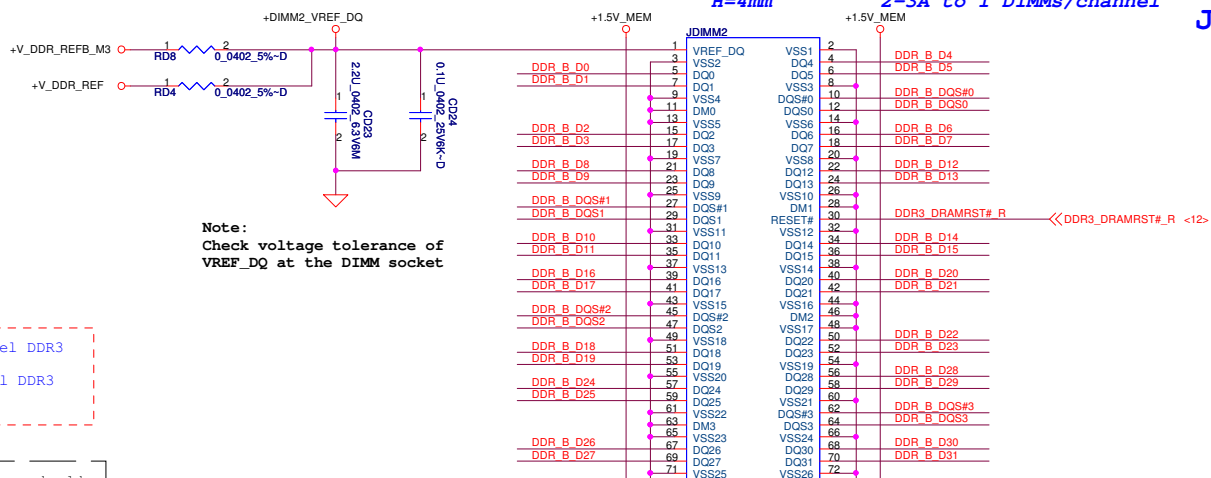


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JDIMMB Reverse Type

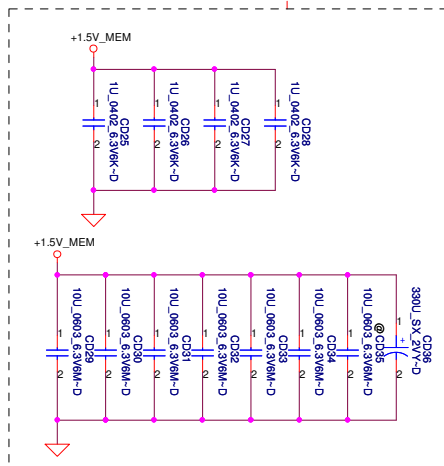


```
Populate RD4, De-Populate RD8 for Intel DDR3
VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3
VREFDQ multiple methods M3
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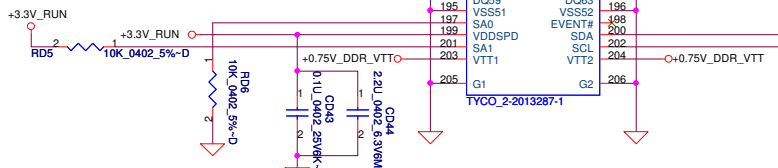
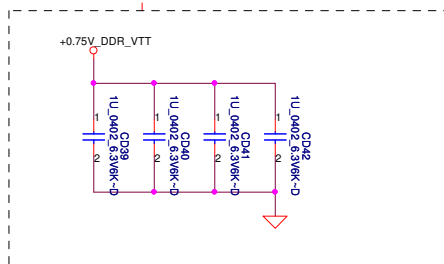
```
<8> DDR_B_DQS#[0..7] << >>
<8> DDR_B_D[0..63] << >>
<8> DDR_B_DQS#[0..7] << >>
<8> DDR_B_MA[0..15] >>
```

All VREF traces should have 10 mil trace width

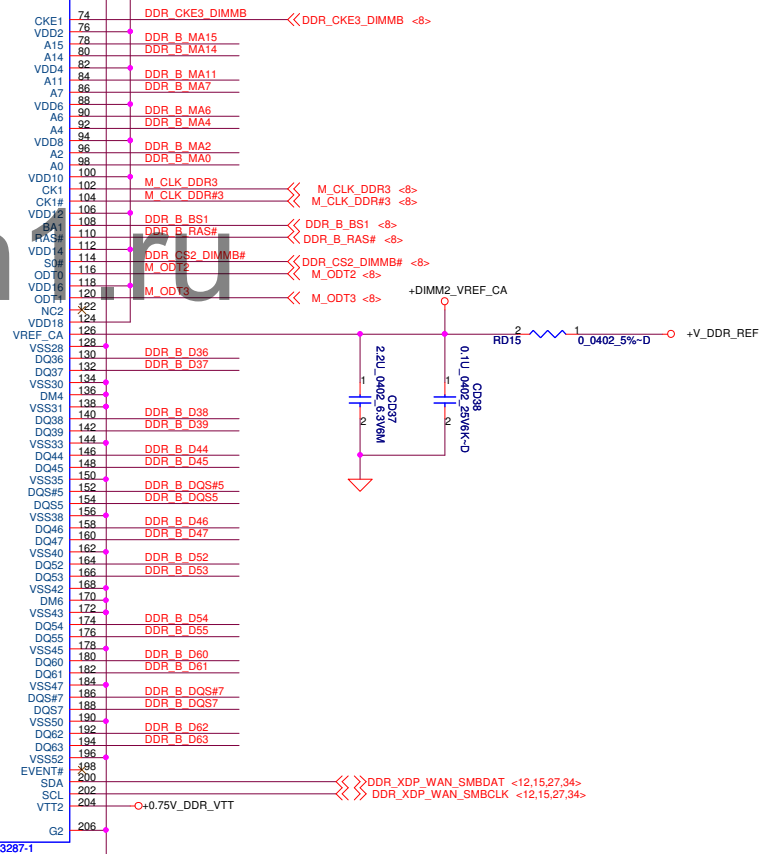
Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2.203,204



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DDRIII-SODIMM SLOT2

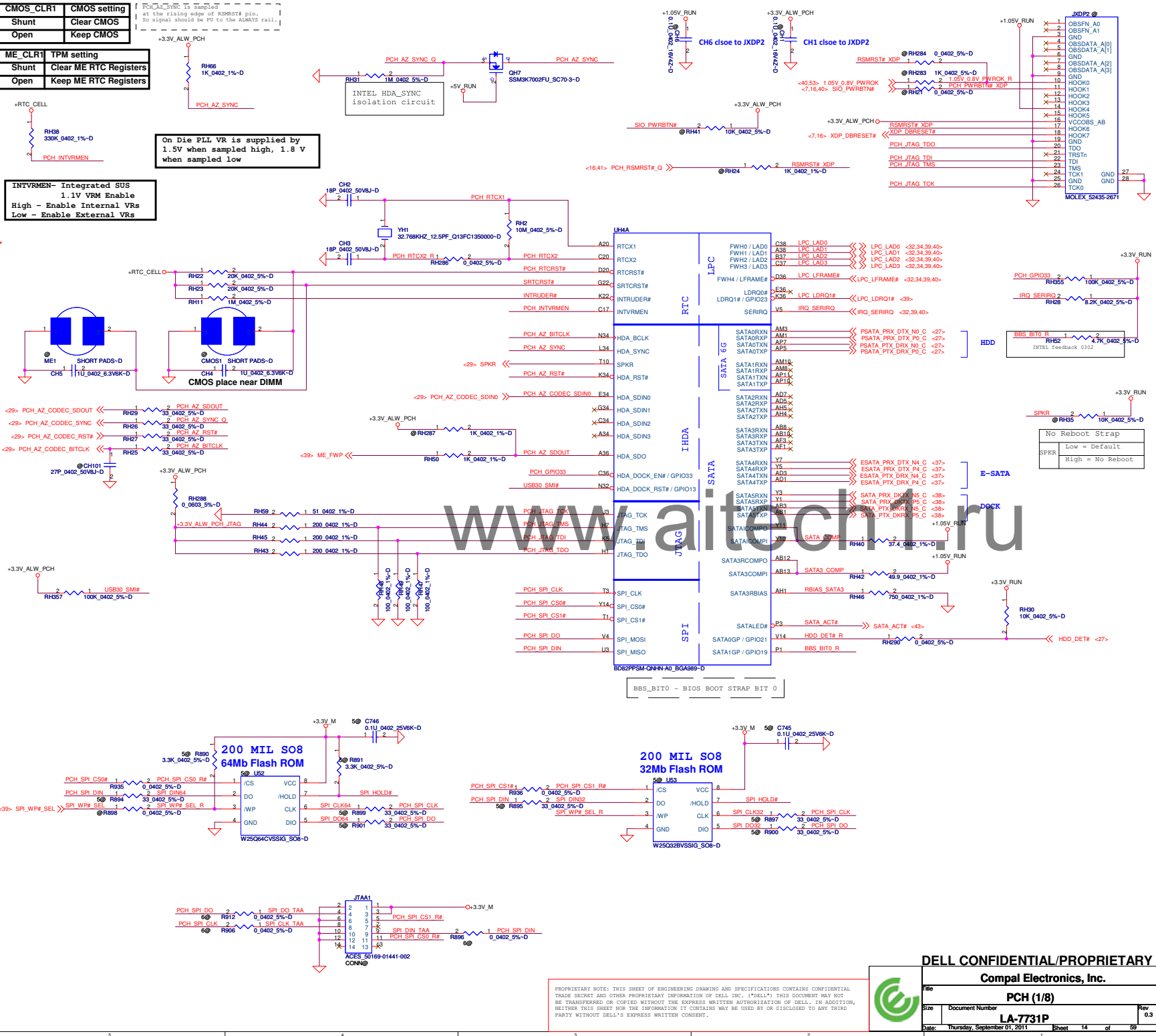
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CMOS CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



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EXPRESS Card---

MMI ---->

10/100/1G LAN ---->

10/100/1G LAN --->

MMI Card--->

PP (Mini Card 3)--->

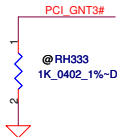
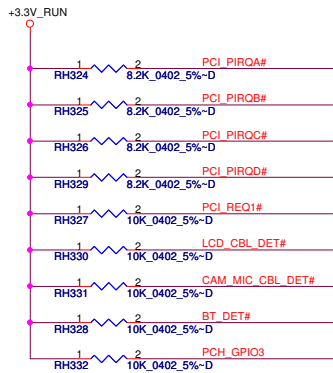
Express card--->

— *Journal of the American Medical Association*

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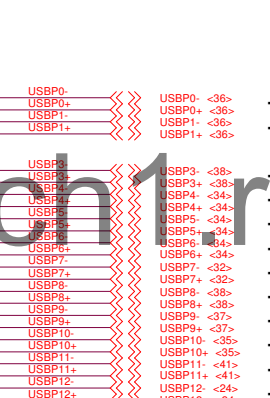
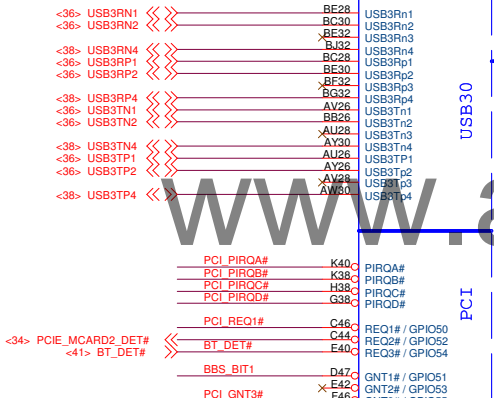
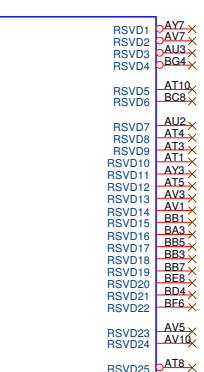
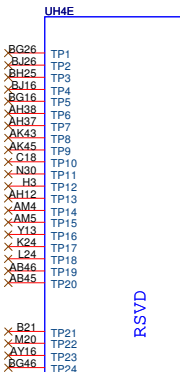
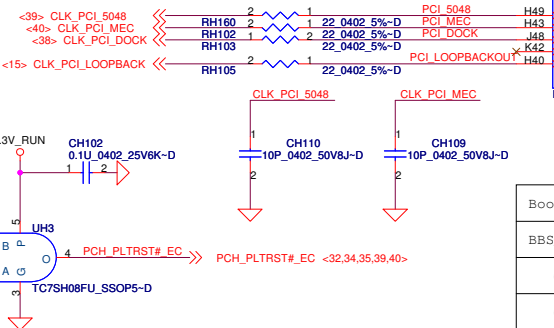


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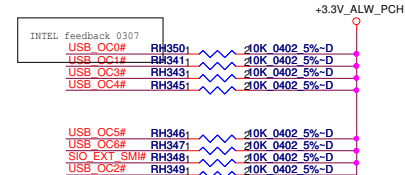


A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

Remove RH335, RH336, RH337, RH338
to save room for D12" only



----->Right Side Top
----->Right Side Bottom
----->MLK DOCK
----->WLAN/WIMAX
----->WWAN/UWB
----->Flash
----->USH
----->DOCK
----->Left side E-SATA
----->Express Card
----->Blue Tooth
----->Camera



Boot BIOS Strap		
BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

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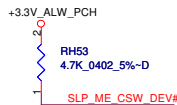
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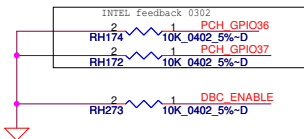
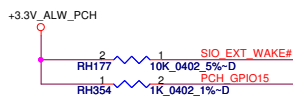
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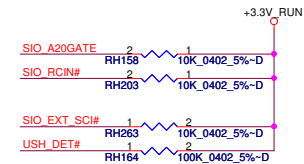
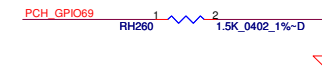
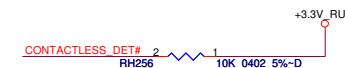
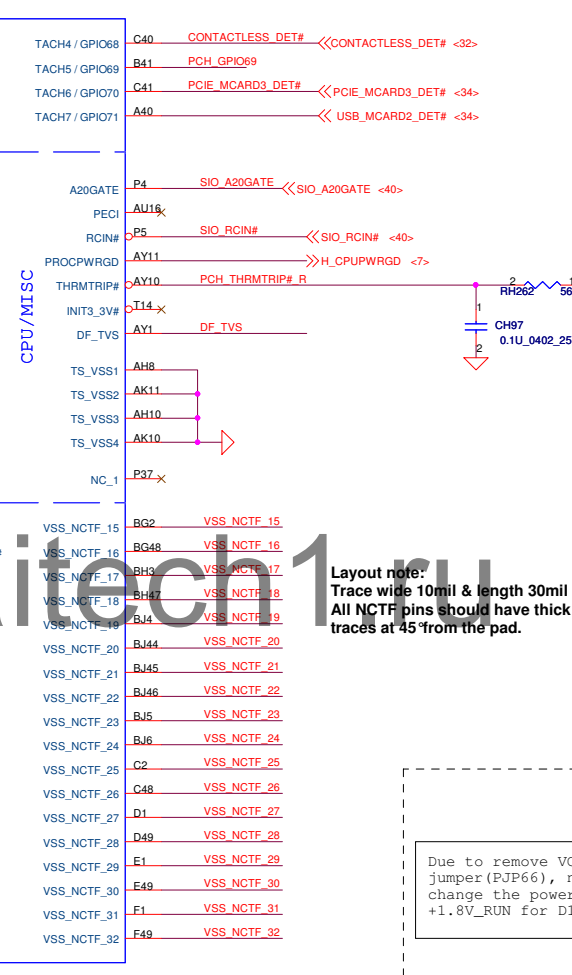
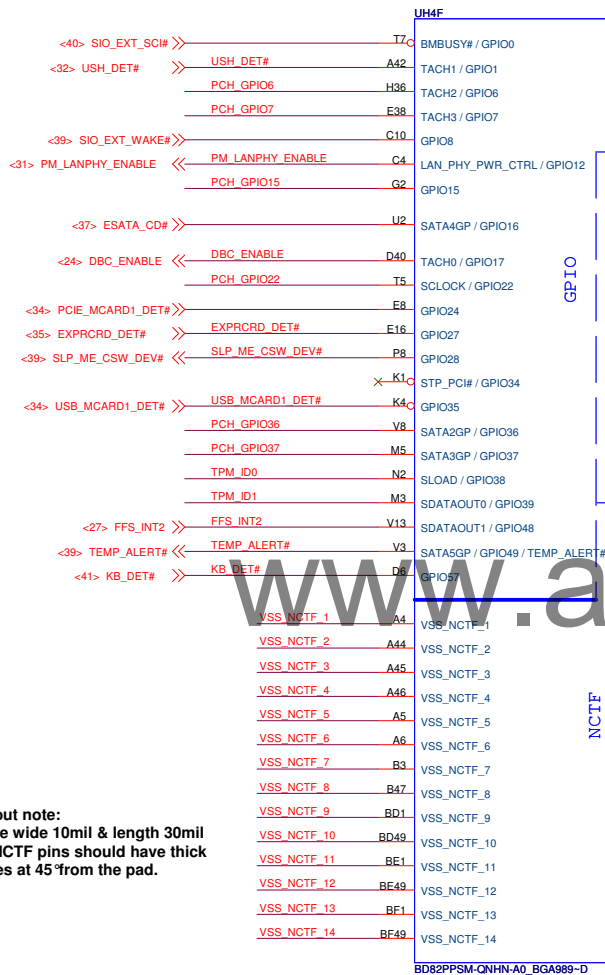
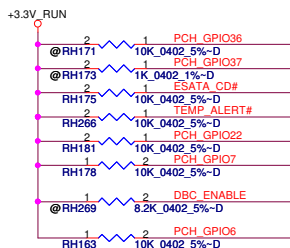
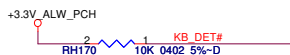
Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

SLP_ME_CSW_DEV# PLL ON DIE VR ENABLE

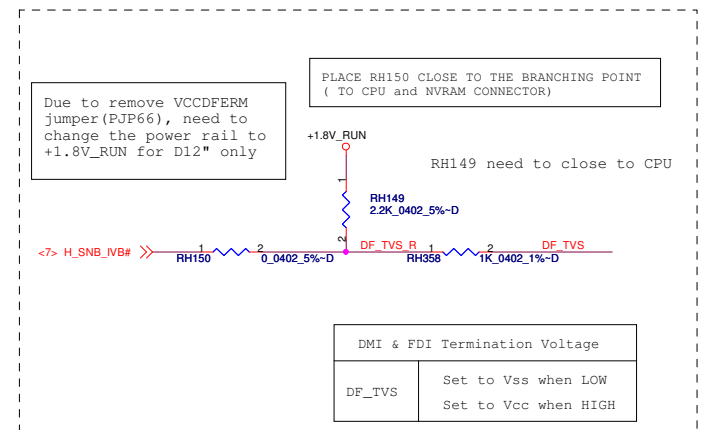
ENABLED - HIGH DEFAULT
DISABLED - LOW



Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



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PCH (5/8)

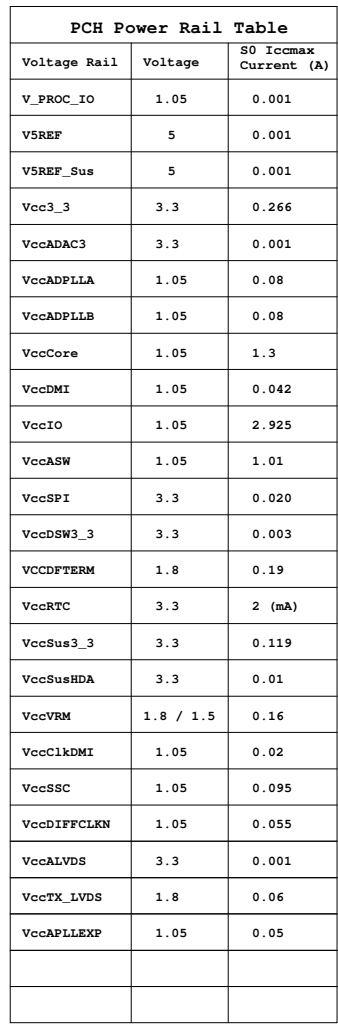
LA-7731P

Rev 0.3

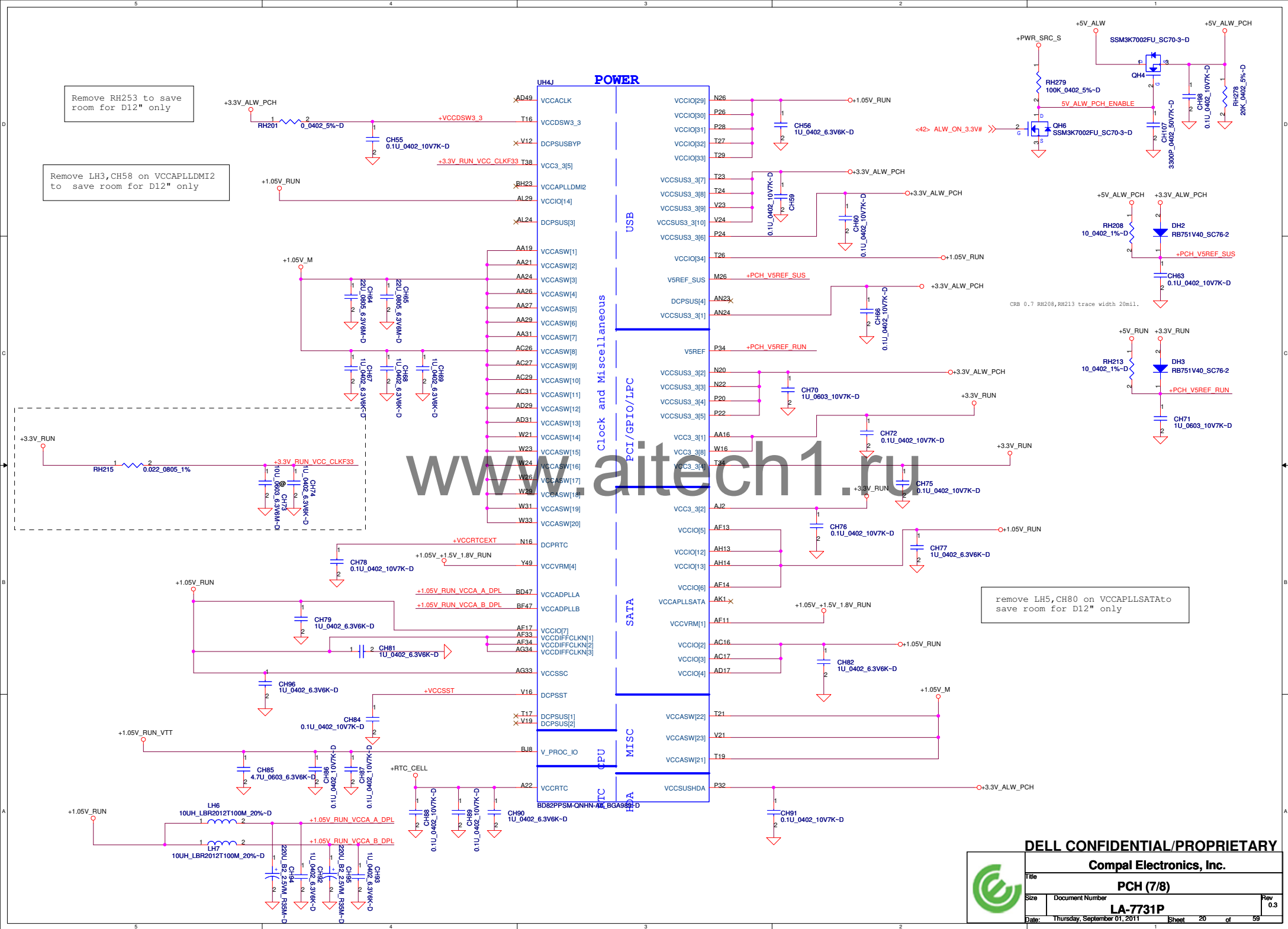
Document Number

Thursday, September 01, 2011

Sheet 18 of 59



PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_FPROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.020
VccDSW3_3	3.3	0.003
VCCDFTerm	1.8	0.19
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.119
VccSusHDA	3.3	0.01
VccVRM	1.8 / 1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKLN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06
VccAPLLEXP	1.05	0.05



UH4H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80] AK38
AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK46
AA33	VSS[4]	VSS[83] AK8
AA34	VSS[5]	VSS[84] AL16
AB11	VSS[6]	VSS[85] AL17
AB14	VSS[7]	VSS[86] AL19
AB39	VSS[8]	VSS[87] AL2
AB4	VSS[9]	VSS[88] AL21
AB43	VSS[10]	VSS[89] AL23
AB5	VSS[11]	VSS[90] AL26
AB7	VSS[12]	VSS[91] AL27
AC19	VSS[13]	VSS[92] AL31
AC2	VSS[14]	VSS[93] AL34
AC21	VSS[15]	VSS[94] AL48
AC24	VSS[16]	VSS[95] AM11
AC33	VSS[17]	VSS[96] AM14
AC34	VSS[18]	VSS[97] AM39
AC48	VSS[19]	VSS[98] AM43
AD10	VSS[20]	VSS[99] AM45
AD11	VSS[21]	VSS[100] AM7
AD12	VSS[22]	VSS[101] AN2
AD13	VSS[23]	VSS[102] AN29
AD24	VSS[24]	VSS[103] AN3
AD26	VSS[25]	VSS[104] AN31
AD27	VSS[26]	VSS[105] AP12
AD33	VSS[27]	VSS[106] AP19
AD34	VSS[28]	VSS[107] AP28
AD36	VSS[29]	VSS[108] AP32
AD37	VSS[30]	VSS[109] AP38
AD38	VSS[31]	VSS[110] AP4
AD39	VSS[32]	VSS[111] AP42
AD4	VSS[33]	VSS[112] AP46
AD40	VSS[34]	VSS[113] AP8
AD42	VSS[35]	VSS[114] AR2
AD43	VSS[36]	VSS[115] AR48
AD45	VSS[37]	VSS[116] AT11
AD46	VSS[38]	VSS[117] AT13
AD8	VSS[39]	VSS[118] AT18
AE2	VSS[40]	VSS[119] AT22
AE3	VSS[41]	VSS[120] AT26
AE4	VSS[42]	VSS[121] AT28
AF10	VSS[43]	VSS[122] AT32
AF12	VSS[44]	VSS[123] AT34
AD14	VSS[45]	VSS[124] AT39
AD16	VSS[46]	VSS[125] AT42
AF16	VSS[47]	VSS[126] AT46
AF19	VSS[48]	VSS[127] AU24
AF24	VSS[49]	VSS[128] AU30
AF26	VSS[50]	VSS[129] AV16
AF27	VSS[51]	VSS[130] AV20
AF29	VSS[52]	VSS[131] AV24
AF31	VSS[53]	VSS[132] AV30
AF38	VSS[54]	VSS[133] AV38
AF4	VSS[55]	VSS[134] AV43
AF42	VSS[56]	VSS[135] AV8
AF5	VSS[57]	VSS[136] AW14
AF7	VSS[58]	VSS[137] AW2
AF8	VSS[59]	VSS[138] AW22
AG19	VSS[60]	VSS[139] AW26
AG2	VSS[61]	VSS[140] AW28
AG3	VSS[62]	VSS[141] AW32
AG31	VSS[63]	VSS[142] AW36
AG48	VSS[64]	VSS[143] AW40
AH11	VSS[65]	VSS[144] AW48
AH3	VSS[66]	VSS[145] AV11
AH36	VSS[67]	VSS[146] AY12
AH39	VSS[68]	VSS[147] AY22
AH40	VSS[69]	VSS[148] AY28
AH42	VSS[70]	
AH46	VSS[71]	
AH7	VSS[72]	
AJ19	VSS[73]	
AJ21	VSS[74]	
AJ24	VSS[75]	
AJ33	VSS[76]	
AJ34	VSS[77]	
AK12	VSS[78]	
AK3	VSS[79]	

BD82PPSM-QNHN-A0_BGA989-D

UH4I		
AY4	VSS[159]	VSS[259] H46
AY42	VSS[160]	VSS[260] K18
AY46	VSS[161]	VSS[261] K26
AY8	VSS[162]	VSS[262] K39
B11	VSS[163]	VSS[263] K46
B15	VSS[164]	VSS[264] K7
B19	VSS[165]	VSS[265] L18
B23	VSS[166]	VSS[266] L2
B27	VSS[167]	VSS[267] L20
B31	VSS[168]	VSS[268] L26
B39	VSS[169]	VSS[269] L38
B7	VSS[170]	VSS[270] L48
F45	VSS[171]	VSS[271] M12
B12	VSS[172]	VSS[272] M18
BB16	VSS[173]	VSS[273] M22
BB20	VSS[174]	VSS[274] M24
BB22	VSS[175]	VSS[275] M30
BB24	VSS[176]	VSS[276] M32
BB28	VSS[177]	VSS[277] M34
BB30	VSS[178]	VSS[278] M38
BB38	VSS[179]	VSS[279] M4
BB4	VSS[180]	VSS[280] M42
BB46	VSS[181]	VSS[281] M46
BC14	VSS[182]	VSS[282] M8
BC18	VSS[183]	VSS[283] N18
BC2	VSS[184]	VSS[284] N24
BC22	VSS[185]	VSS[285] P11
BC26	VSS[186]	VSS[286] P18
BC32	VSS[187]	VSS[287] P30
BC34	VSS[188]	VSS[288] P40
BC36	VSS[189]	VSS[289] P43
BC40	VSS[190]	VSS[290] P47
BC42	VSS[191]	VSS[291] P7
BC46	VSS[192]	VSS[292] R2
BC48	VSS[193]	VSS[293] R48
BD46	VSS[194]	VSS[294] T12
BD5	VSS[195]	VSS[295] T31
BE22	VSS[196]	VSS[296] T37
BE26	VSS[197]	VSS[297] T4
BE40	VSS[198]	VSS[298] W34
BF10	VSS[199]	VSS[299] T46
BF12	VSS[200]	VSS[300] T8
BF16	VSS[201]	VSS[301] V11
BF20	VSS[202]	VSS[302] V17
BF24	VSS[203]	VSS[303] V26
BF26	VSS[204]	VSS[304] V27
BF28	VSS[205]	VSS[305] V29
BD3	VSS[206]	VSS[306] V31
BF30	VSS[207]	VSS[307] V38
BF38	VSS[208]	VSS[308] W17
BF40	VSS[209]	VSS[309] W19
BF42	VSS[210]	VSS[310] W2
BF46	VSS[211]	VSS[311] W27
BF48	VSS[212]	VSS[312] W48
BF49	VSS[213]	VSS[313] Y12
BF53	VSS[214]	VSS[314] Y4
BG44	VSS[215]	VSS[315] Y42
BG46	VSS[216]	VSS[316] Y46
BG47	VSS[217]	VSS[317] Y8
BG48	VSS[218]	VSS[318] Y29
BG49	VSS[219]	VSS[319] N24
BG53	VSS[220]	VSS[320] N24
BG54	VSS[221]	VSS[321] N24
BG55	VSS[222]	VSS[322] N24
BG56	VSS[223]	VSS[323] N24
BG57	VSS[224]	VSS[324] N24
BG58	VSS[225]	VSS[325] N24
BG59	VSS[226]	VSS[326] N24
BG60	VSS[227]	VSS[327] N24
BG61	VSS[228]	VSS[328] N24
BG62	VSS[229]	VSS[329] N24
BG63	VSS[230]	VSS[330] N24
BG64	VSS[231]	VSS[331] N24
BG65	VSS[232]	VSS[332] N24
BG66	VSS[233]	VSS[333] N24
BG67	VSS[234]	VSS[334] N24
BG68	VSS[235]	VSS[335] N24
BG69	VSS[236]	VSS[336] N24
BG70	VSS[237]	VSS[337] N24
BG71	VSS[238]	VSS[338] N24
BG72	VSS[239]	VSS[339] N24
BG73	VSS[240]	VSS[340] N24
BG74	VSS[241]	VSS[341] N24
BG75	VSS[242]	VSS[342] N24
BG76	VSS[243]	VSS[343] N24
BG77	VSS[244]	VSS[344] N24
BG78	VSS[245]	VSS[345] N24
BG79	VSS[246]	VSS[346] N24
BG80	VSS[247]	VSS[347] N24
BG81	VSS[248]	VSS[348] N24
BG82	VSS[249]	VSS[349] N24
BG83	VSS[250]	VSS[350] N24
BG84	VSS[251]	VSS[351] N24
BG85	VSS[252]	VSS[352] N24
BG86	VSS[253]	
BG87	VSS[254]	
BG88	VSS[255]	
BG89	VSS[256]	
BG90	VSS[257]	
BG91	VSS[258]	
BG92	VSS[259]	

BD82PPSM-QNHN-A0_BGA989-D

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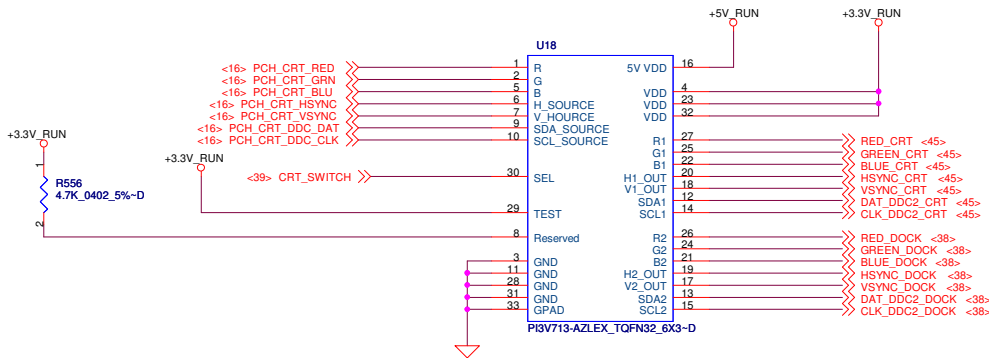


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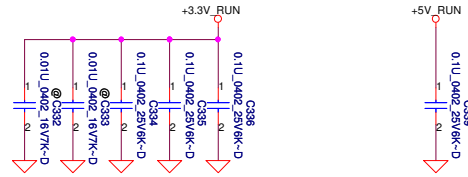
Compal Electronics, Inc.

Title			PCH (8/8)
Size	Document Number	Rev	0.3
LA-7731P			
Date	Thursday, September 01, 2011	Sheet	21 of 59

SW for MB/DOCK



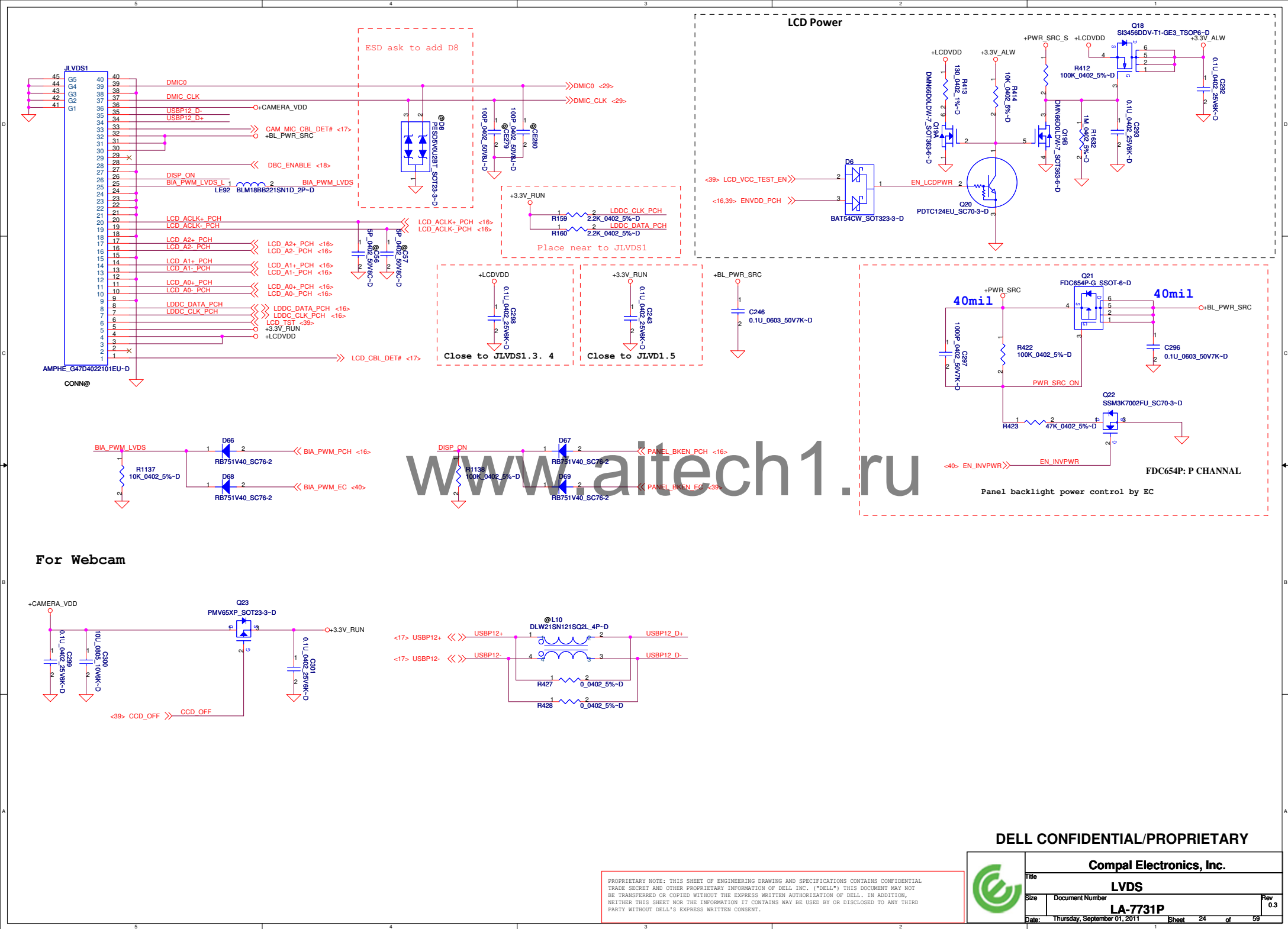
SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



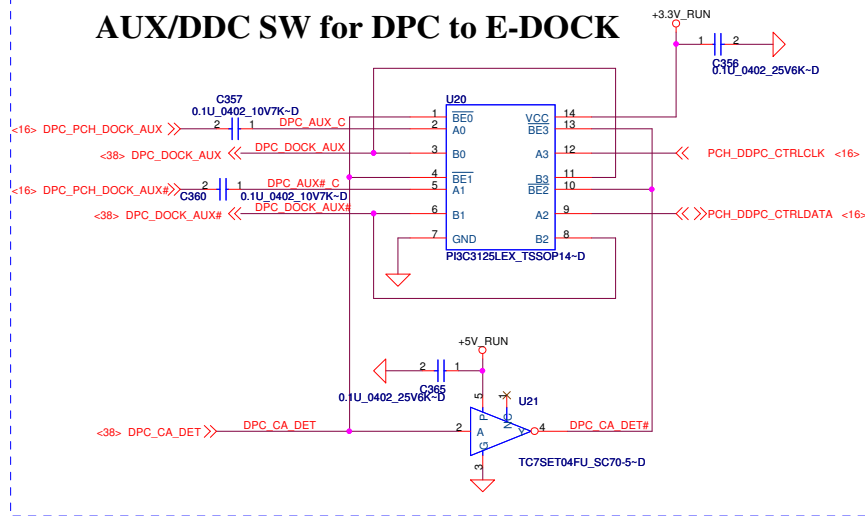
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Compal Electronics, Inc.			
Title CRT/Video switch			
Size	Document Number		Rev
	LA-7731P		0.3
Date:	Thursday, September 01, 2011	Sheet	23 of 59

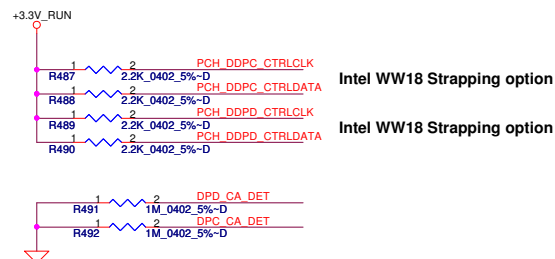
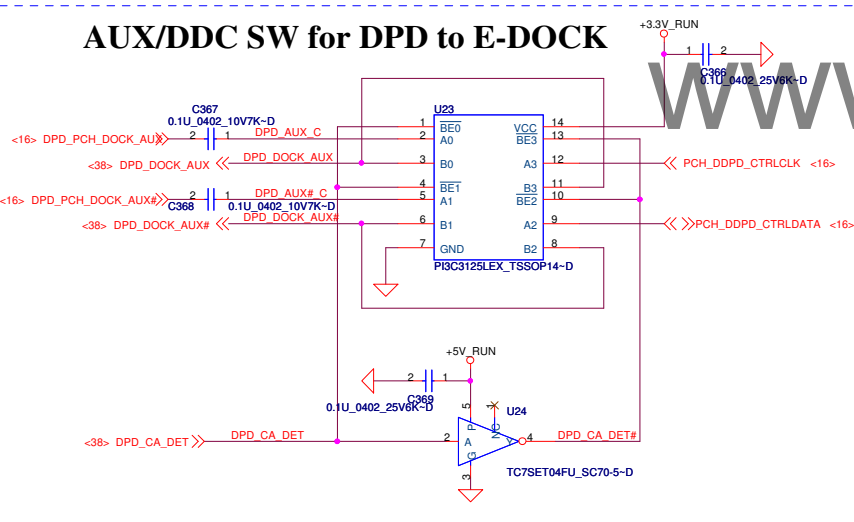


AUX/DDC SW for DPC to E-DOCK



There is a new die for PI3C3125. Sample available on May.

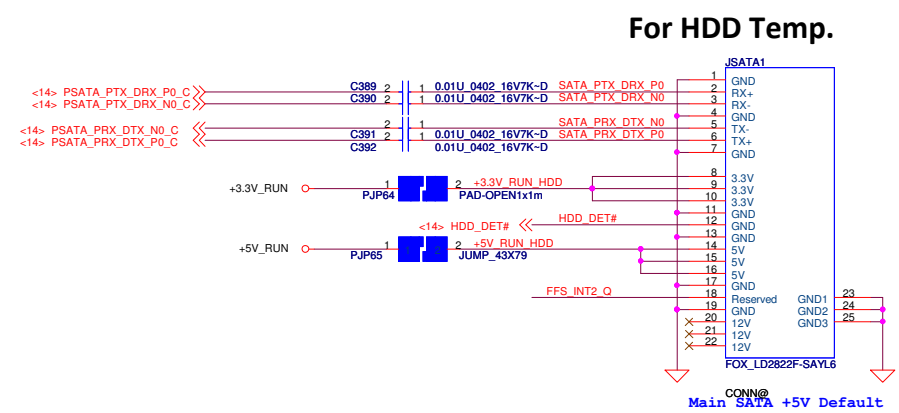
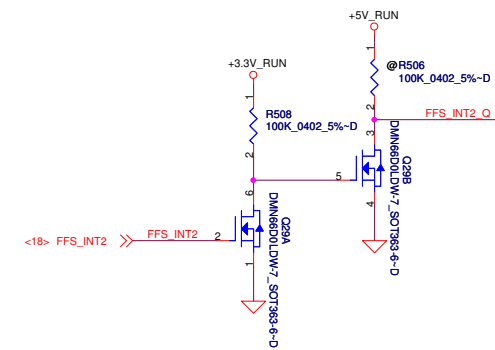
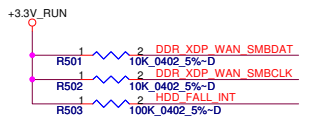
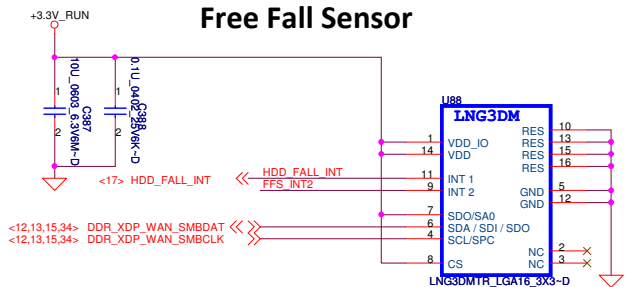
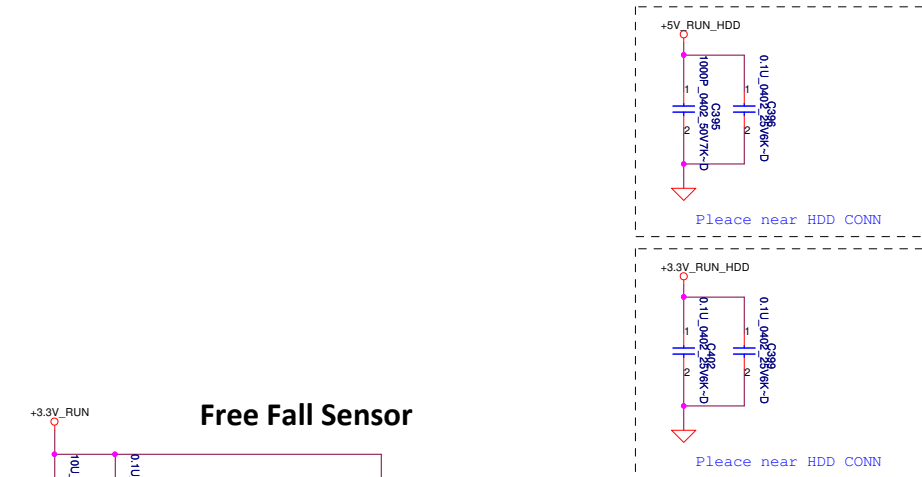
AUX/DDC SW for DPD to E-DOCK



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Compal Electronics, Inc.

HDD CONNECTOR

LA-7731P

Date: Thursday, September 01, 2011 Sheet 27 of 59

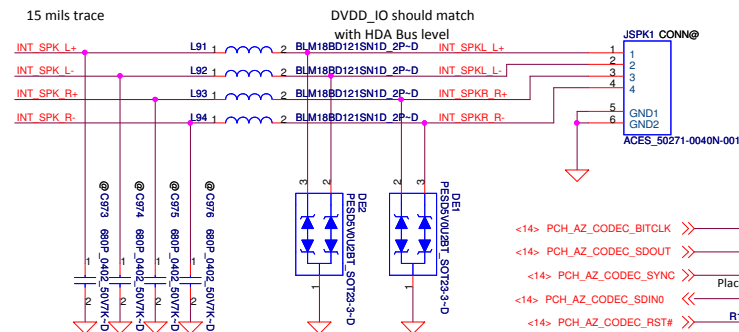
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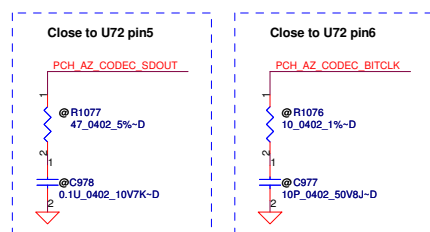


DELL CONFIDENTIAL/PROPRIETARY			
Compal Electronics, Inc.			
Title		ODD CONNECTOR	
Size	Document Number	LA-7731P	Rev 0.3
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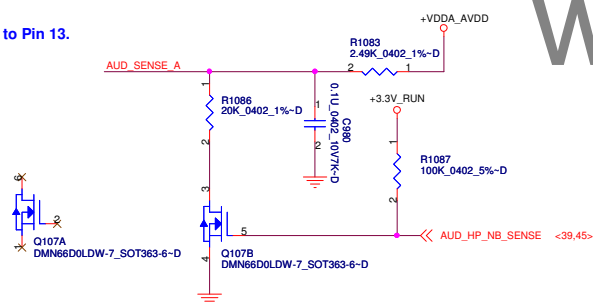
Internal Speakers Header



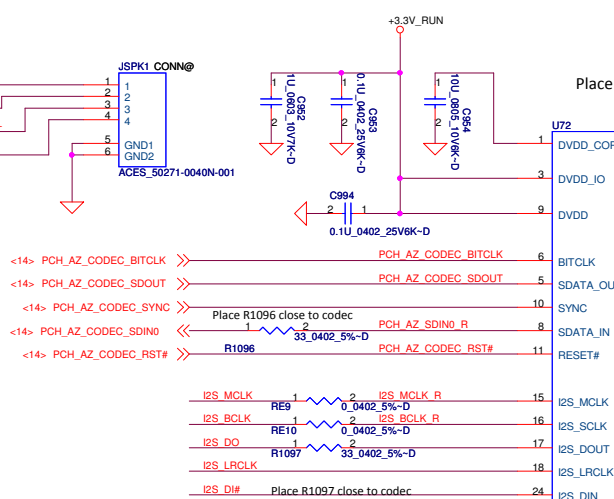
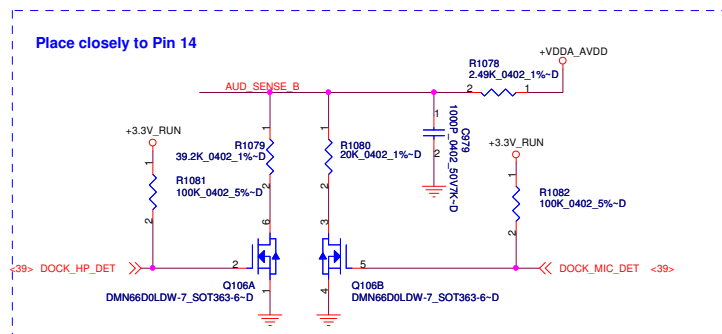
ESD ask to add DE1,DE2



Place closely to Pin 13.

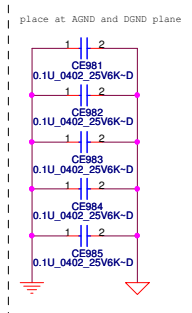


Place closely to Pin 14



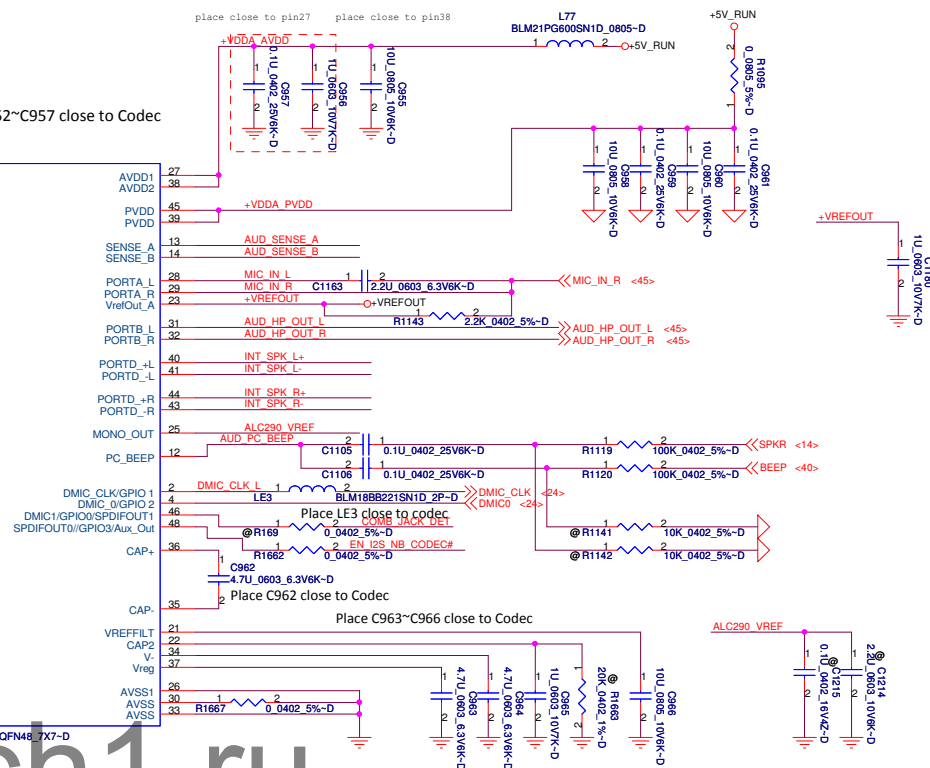
BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

EMI request to add C984,C985

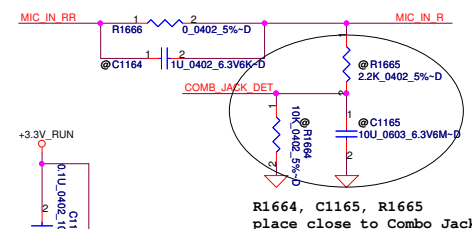
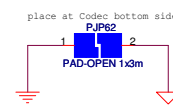


PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Intel
PORT D	Internal SPK
PORT E	DOCK
PORT F	DOCK

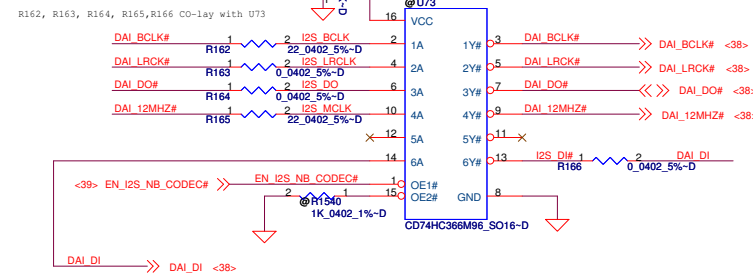
Place C994, C952~C957 close to Codec



Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals



R1664, C1165, R1665
place close to Combo Jack



Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

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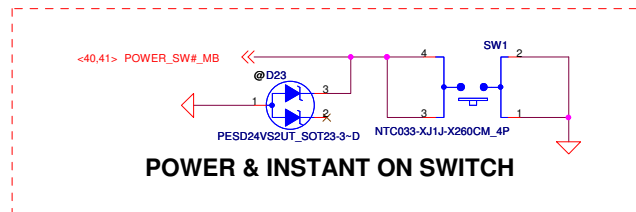
Azalia (HD) Codec

LA-7731B

LA-7731F

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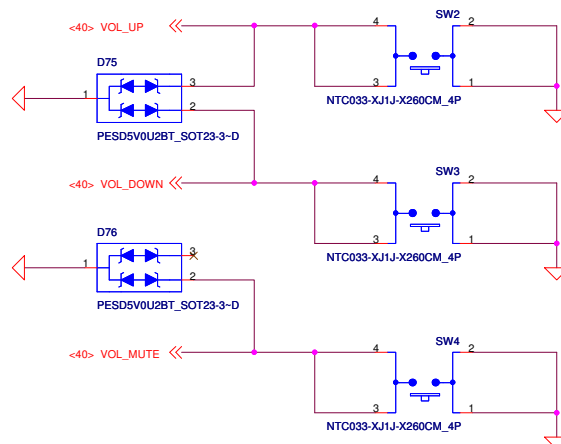
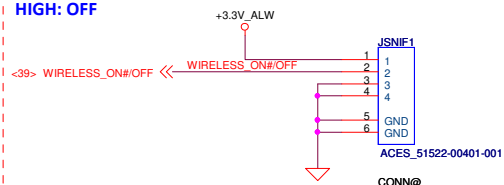
Rev
0.3



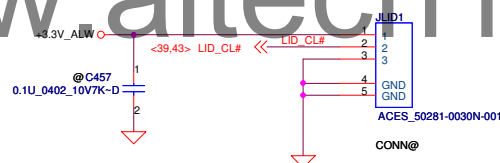
POWER & INSTANT ON SWITCH

Default on,
WIRELESS_ON/OFF#:
LOW: ON
HIGH: OFF

Sniffer Board



Lid board



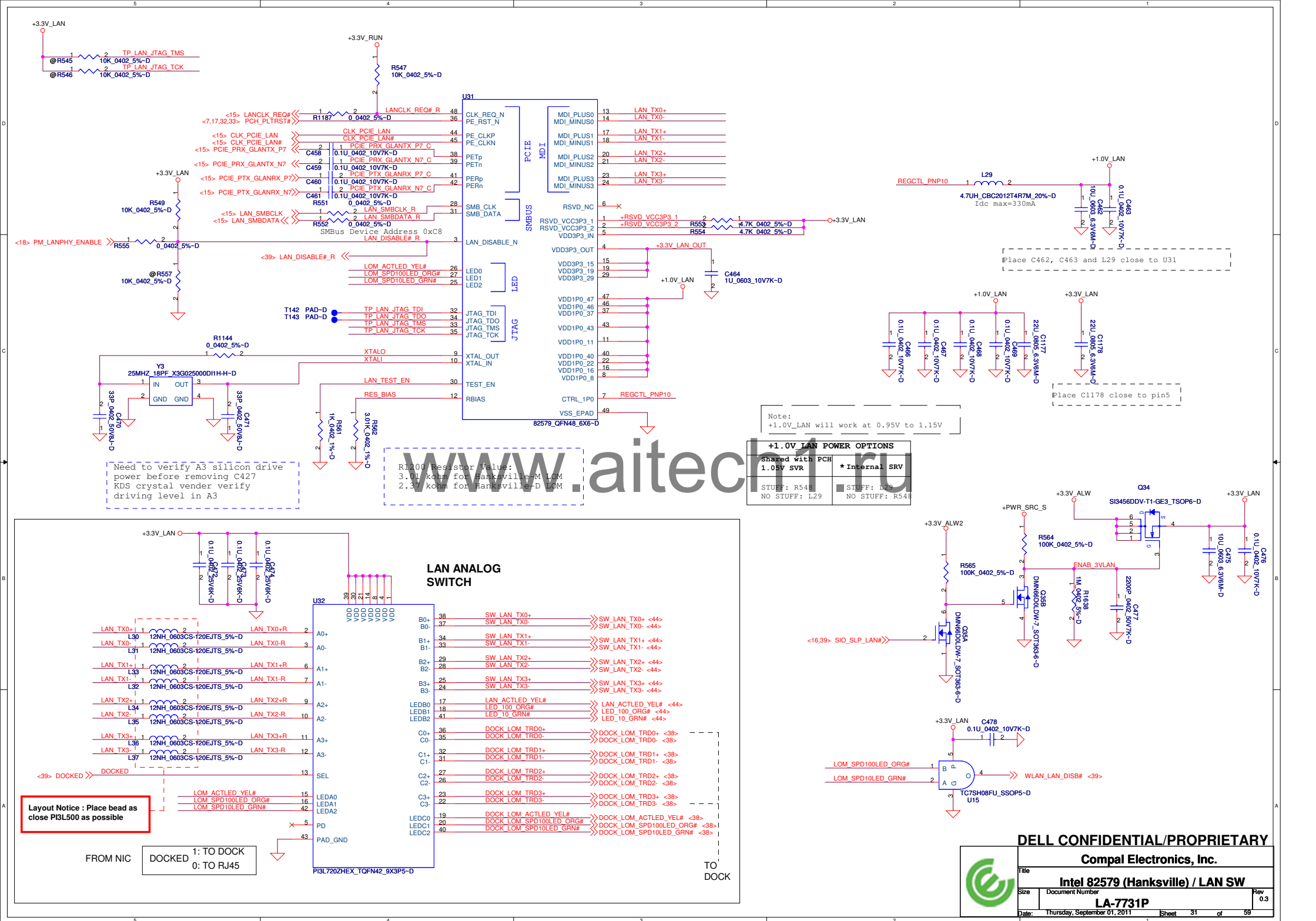
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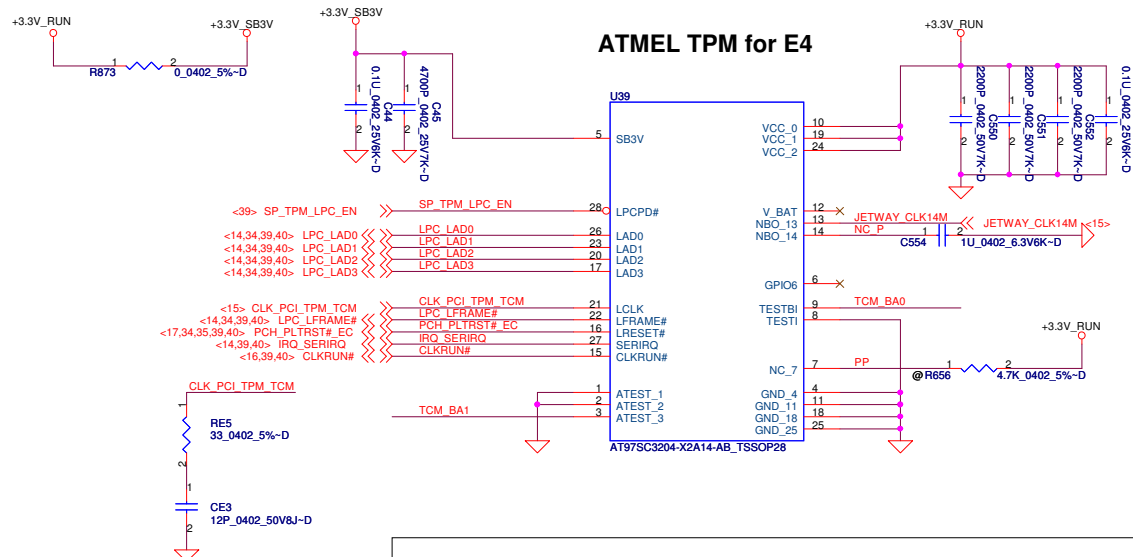
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Title	PWR SW/Sub-board Connector		
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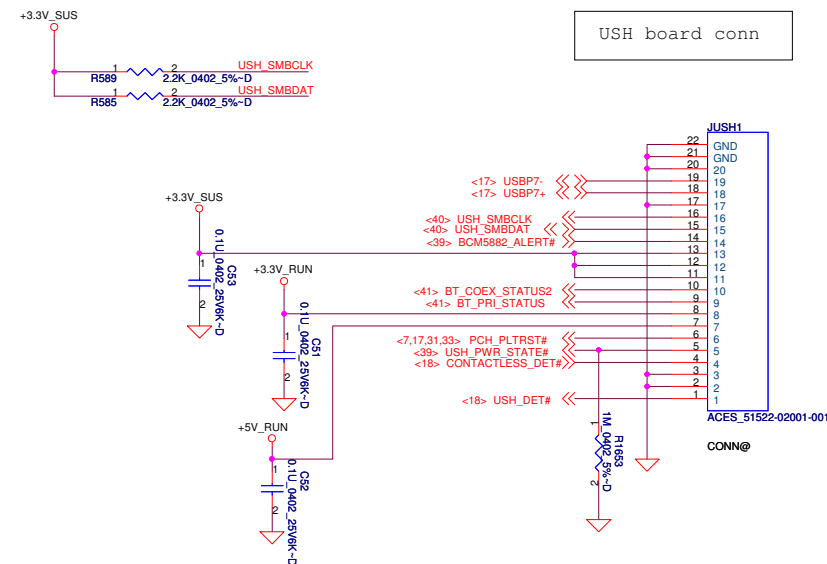
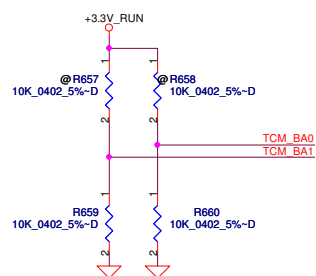
Co-lay U37 and U39

LPC layout: Place TCM first and then end LPC with TPM.

China TCM: NationZ & Jetway co-lay

LOW:Power Down Mode

High:Working Mode

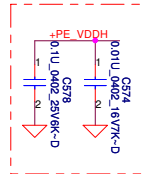


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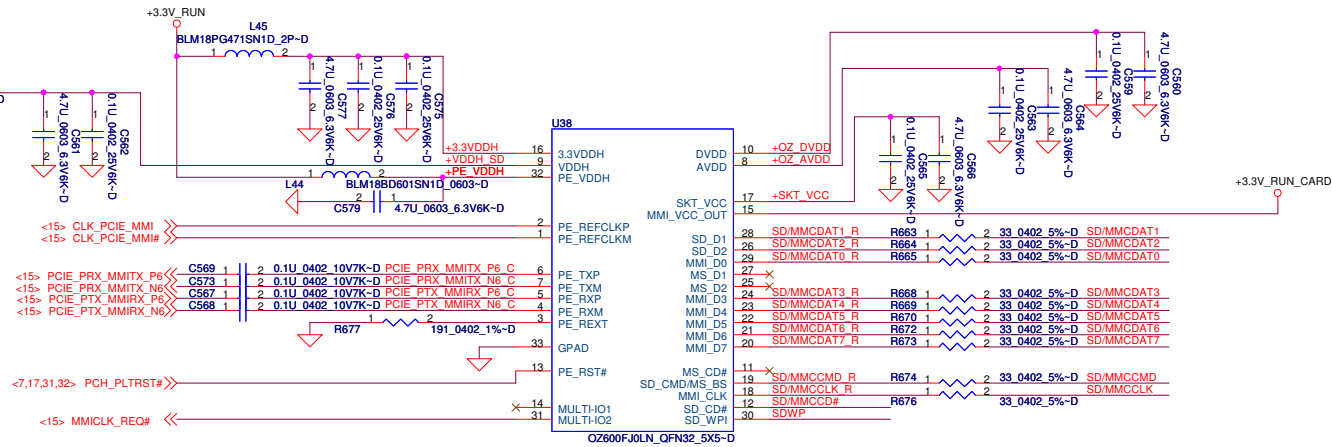
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TPM/TCM			
Size	Document Number	Rev	
	LA-7731P	0.3	
Date:	Thursday, September 01, 2011	Sheet	32 of 59

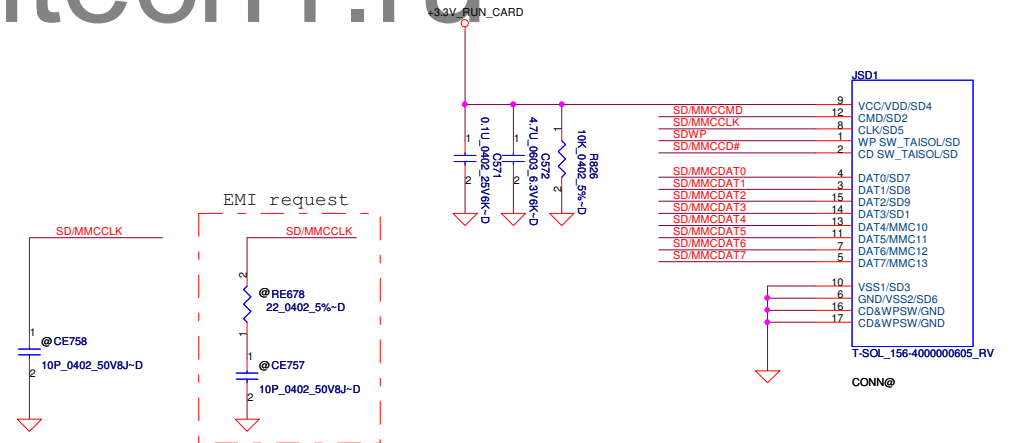
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place close to pin U38.32



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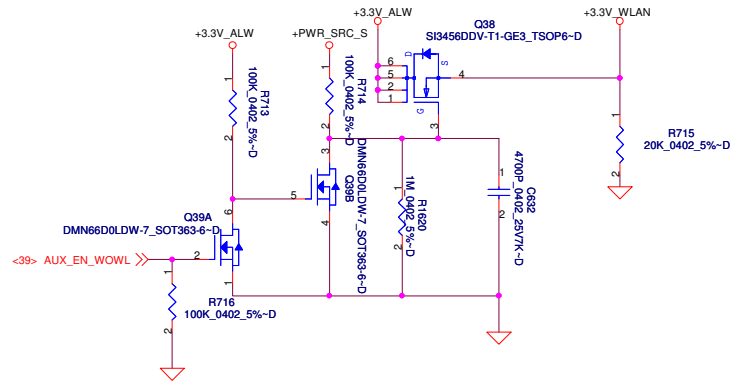


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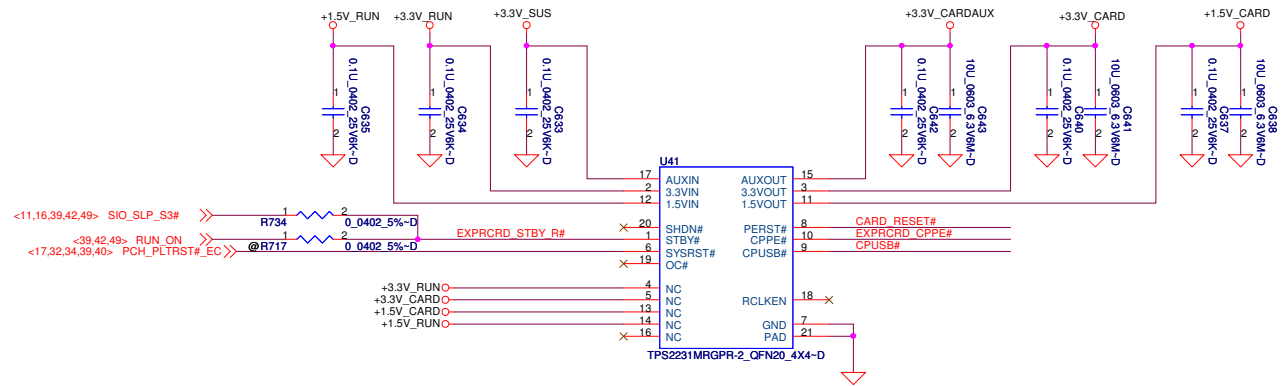
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Card Reader			
Title	LA-7731P		
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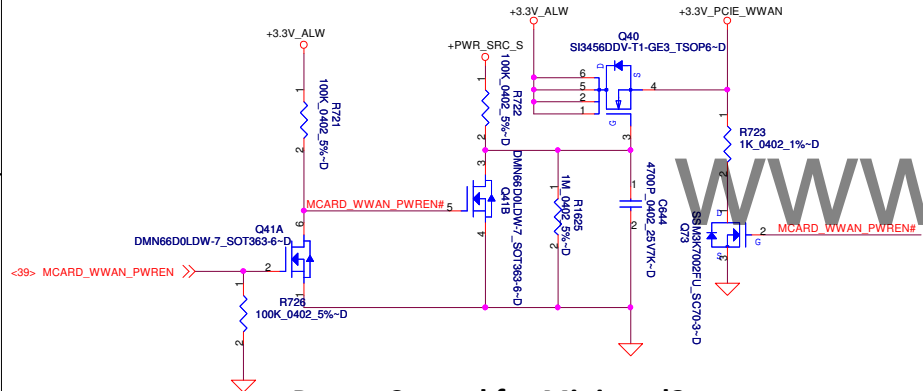
Power Control for Mini card1



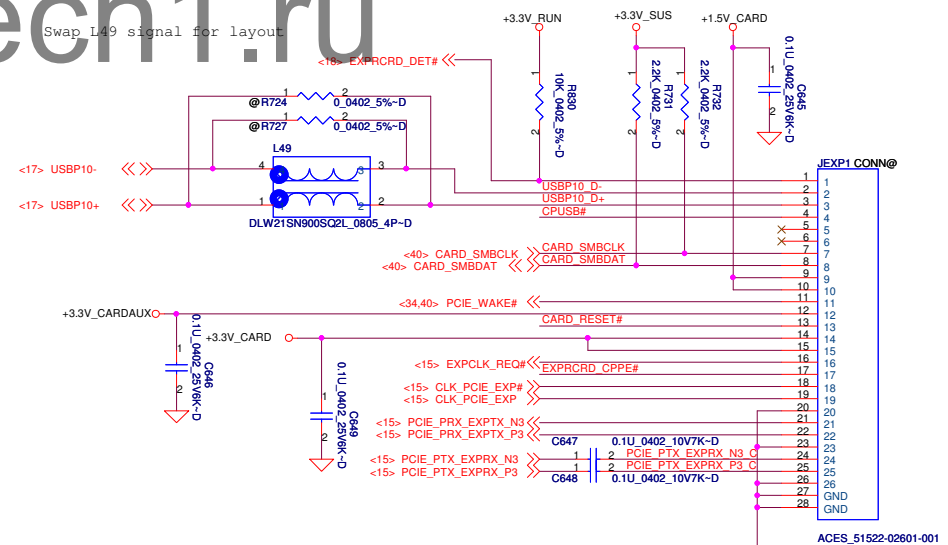
Express Card PWR S/W



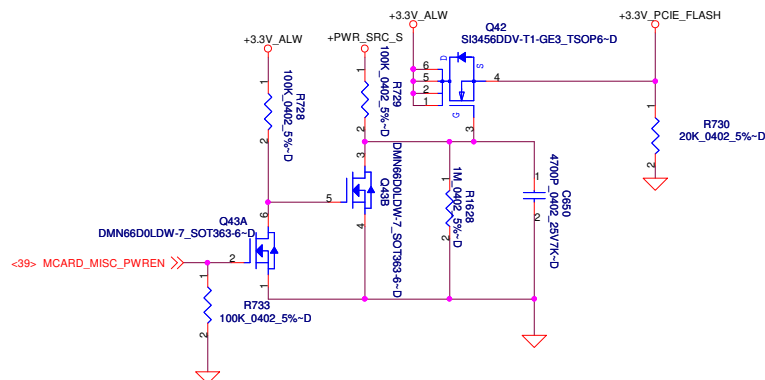
Power Control for Mini card2



Express Card Conn.



Power Control for Mini card3



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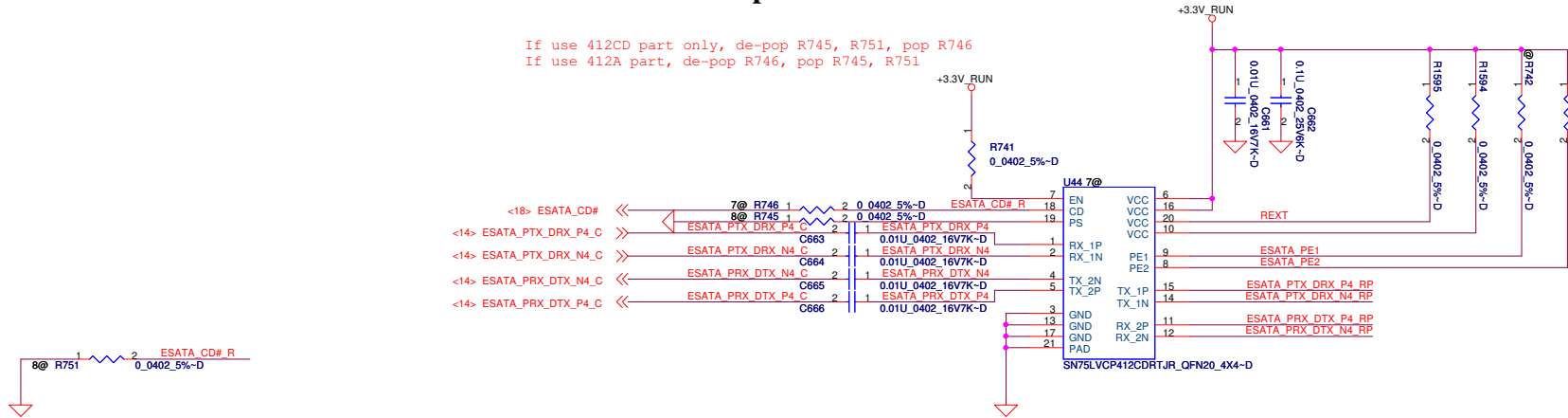
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PCIE-SATA SW / PCIE PWR		
Size	Document Number	Rev
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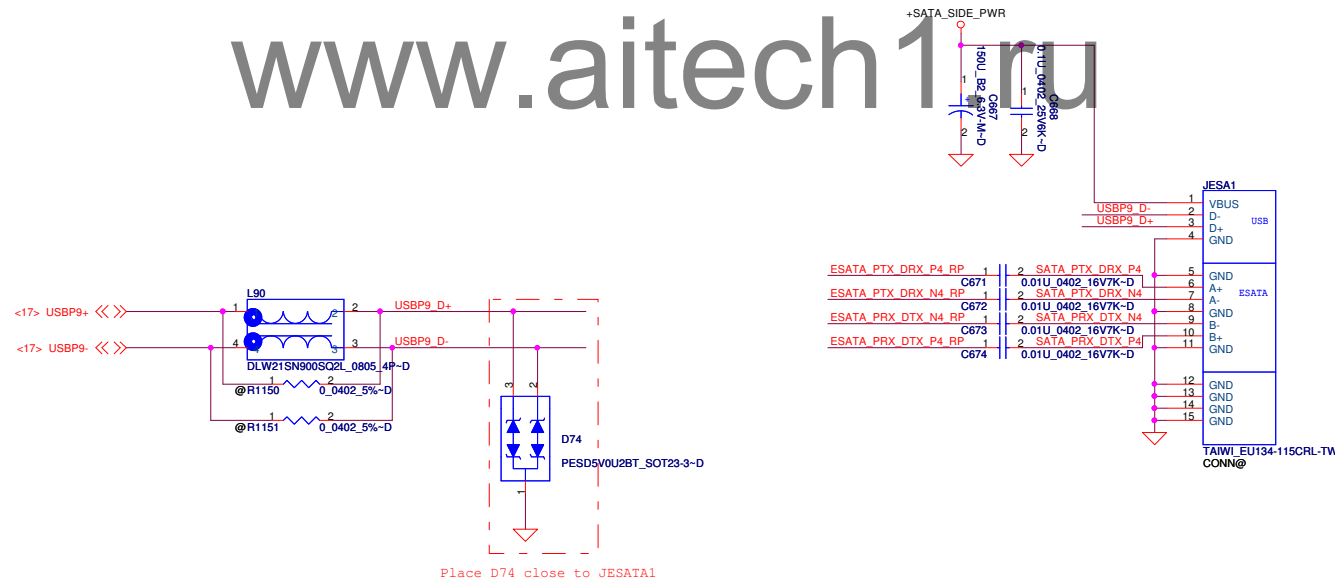
ESATA Repeater

If use 412CD part only, de-pop R745, R751, pop R746
If use 412A part, de-pop R746, pop R745, R751

8@ U44
PS8513BTQFN20GTR-A0
SA00004WR00



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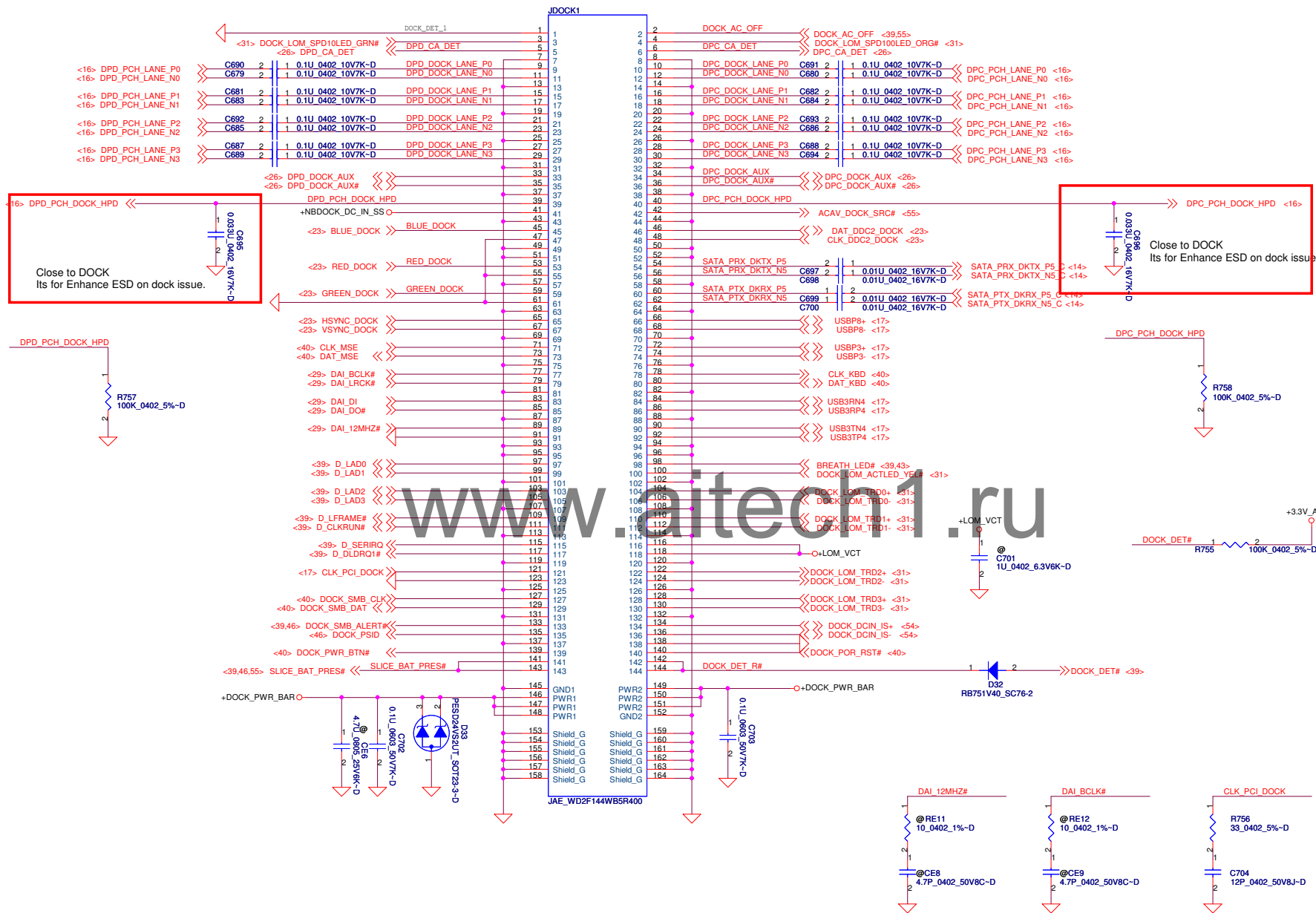
Place D74 close to JESATA1

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Title			
USB/ESATA/IO/MDC			
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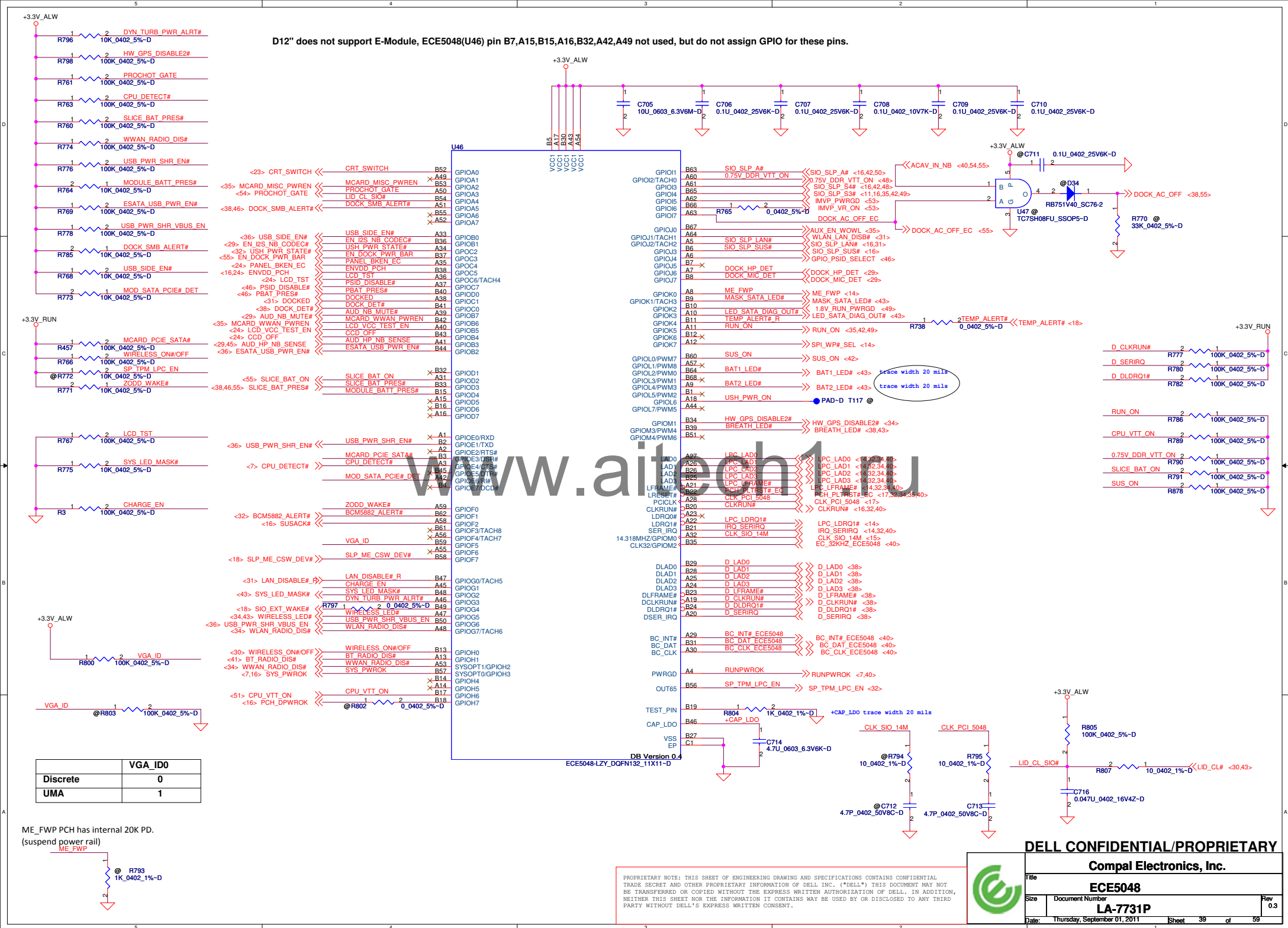
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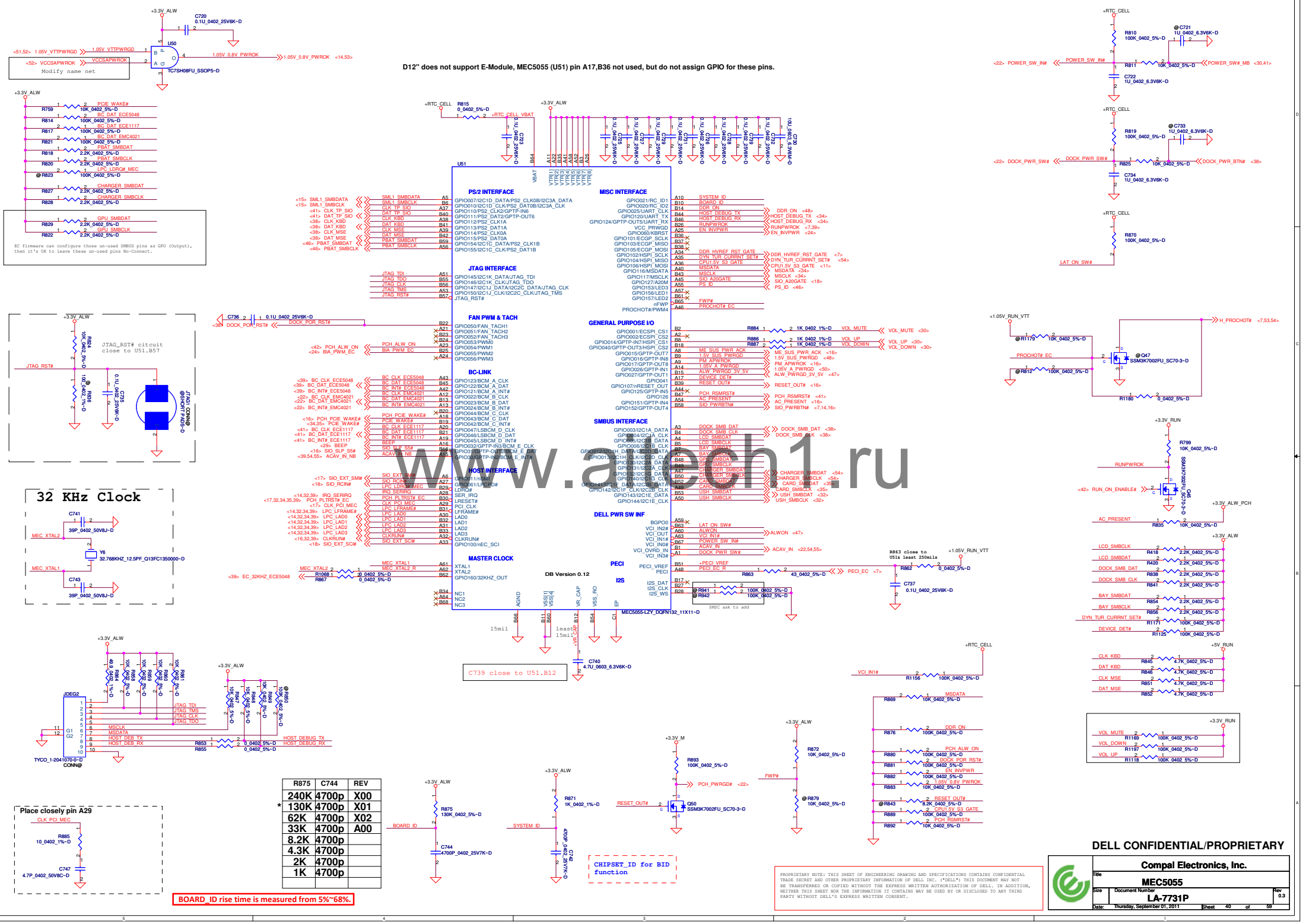


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D12" does not support E-Module, MEC5055 (U51) pin A17,B36 not used, but do not assign GPIO for these pins.

R875	C744	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	A00
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%-68%.

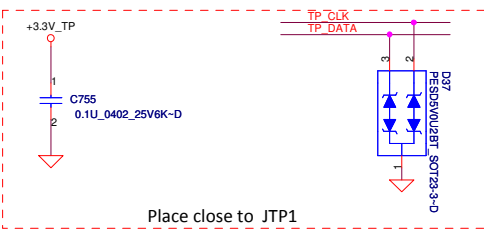
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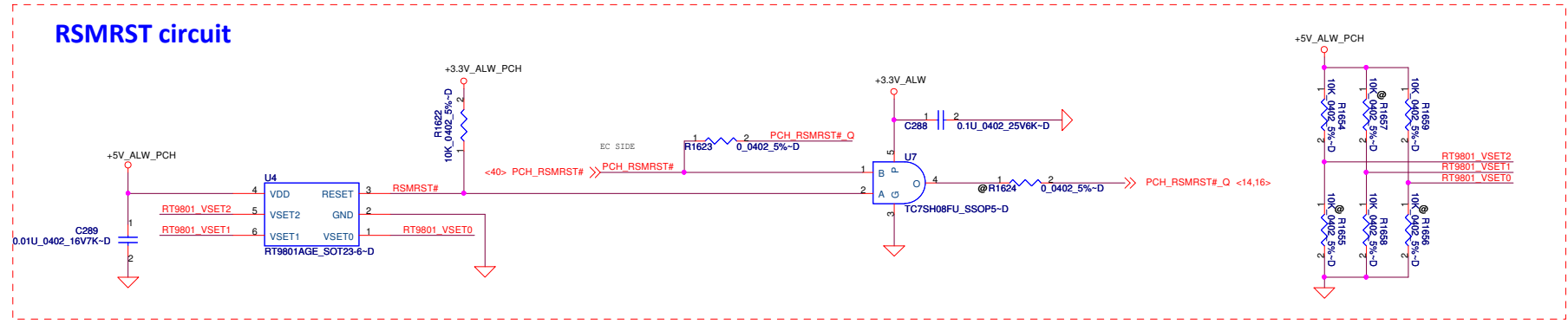
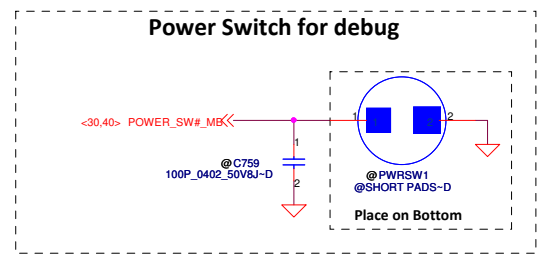
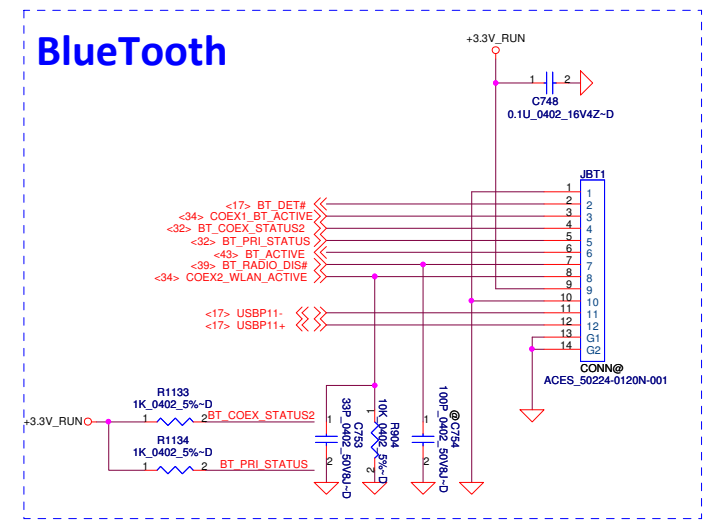
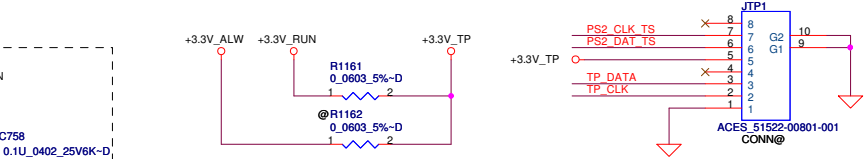
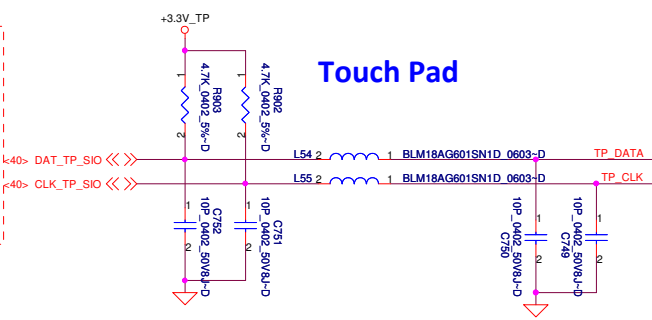
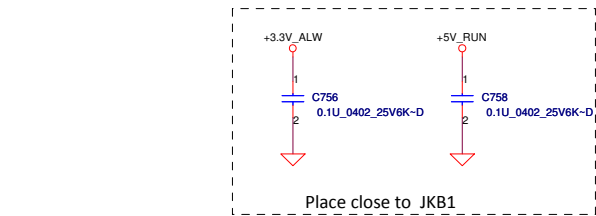
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D37 ESD ask to change to SOT23-3

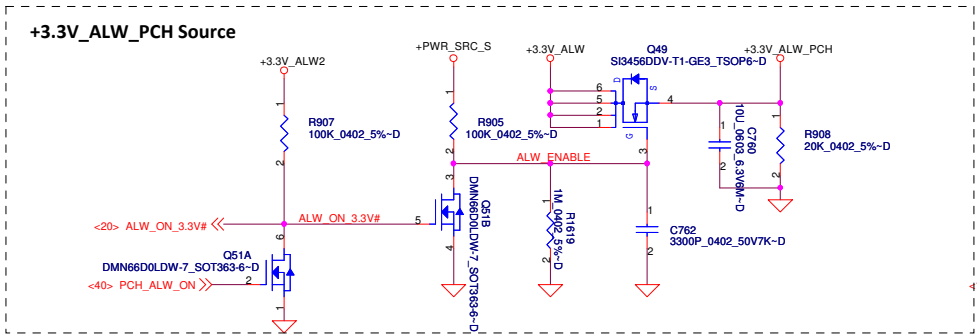


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+3.3V_ALW_PCH Source

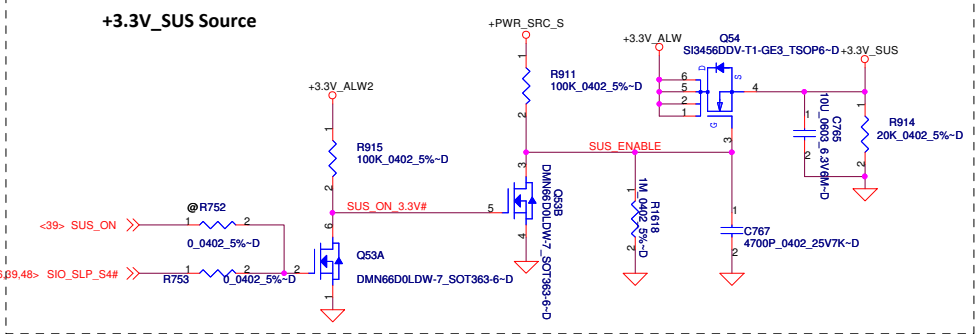
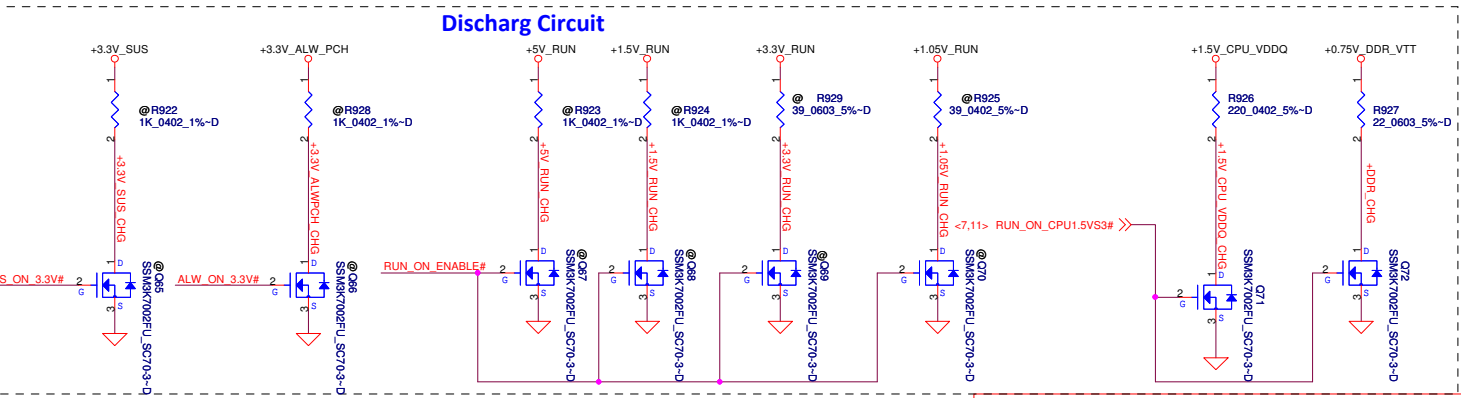
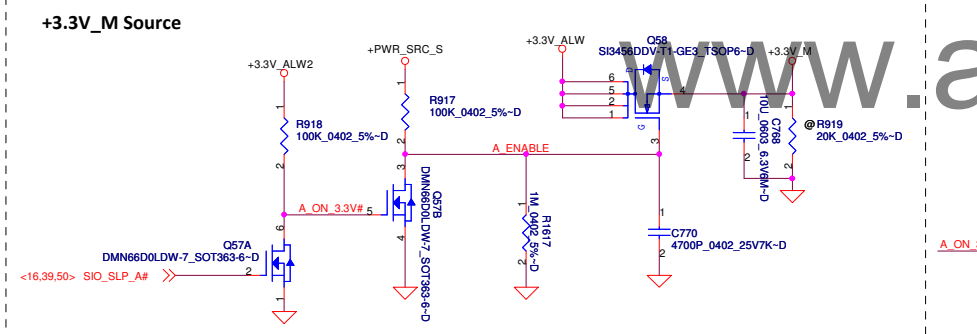
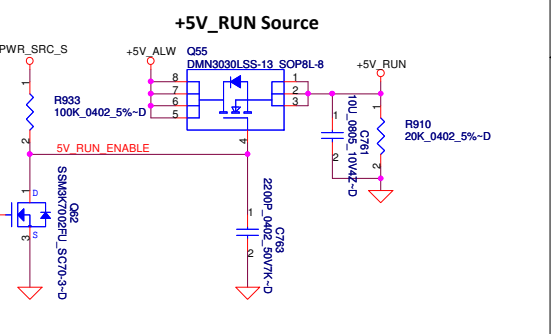
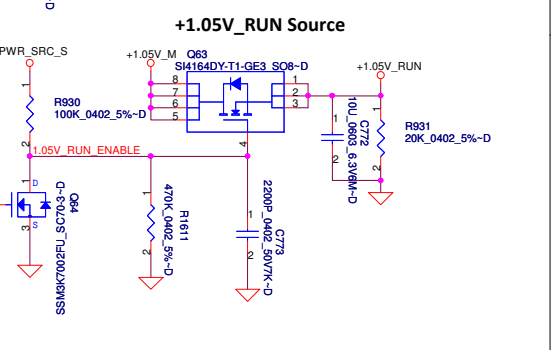
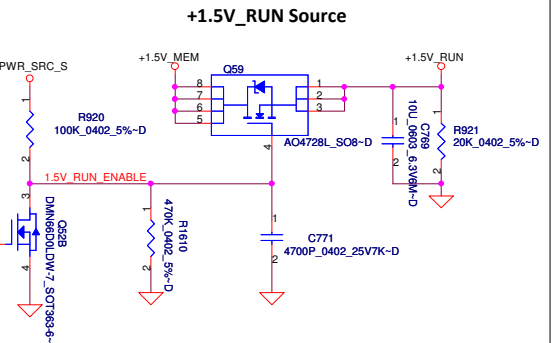
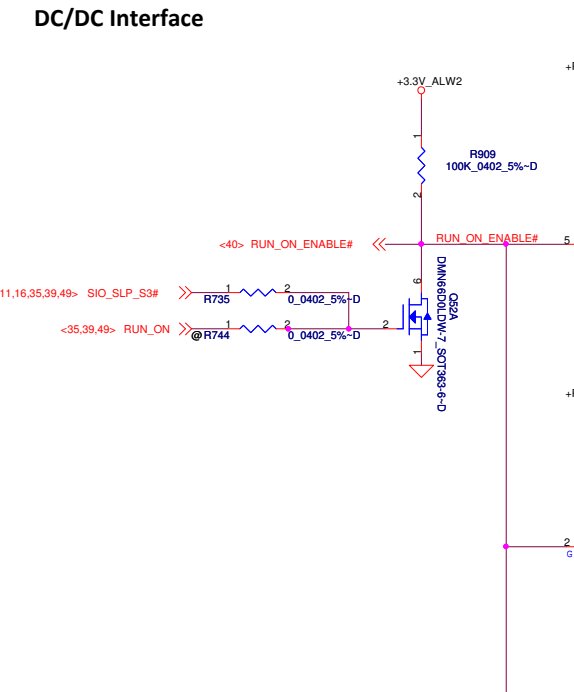
The schematic diagram illustrates the +3.3V_ALW_PCH Source circuit. Key components and connections include:

- Inputs:** +3.3V_ALW2, +PWR_SRC_S, and +3.3V_ALW.
- Resistors:**
 - R907 (100K_0402_5%-D) connected to +3.3V_ALW2.
 - R905 (100K_0402_5%-D) connected to +PWR_SRC_S.
 - R1619 (1M_0402_5%-D) connected to +3.3V_ALW.
 - R908 (20K_0402_5%-D) connected to +3.3V_ALW_PCH.
- MOSFETs:**
 - Q51A (DMN66D0LDW-7_SOT3636-D) is a P-channel MOSFET with its gate connected to ALW_ON_3.3V# and its source to ground.
 - Q49 (SI43456DDV-T1-GE3_TSOP6-D) is an N-channel MOSFET with its gate connected to ALW_ENABLE and its source to ground.
- Diode:** C762 (3300P_0402_50V7K-D) is connected in series with the output line.
- Outputs:** ALW_ON_3.3V# and PCH_ALW_ON.



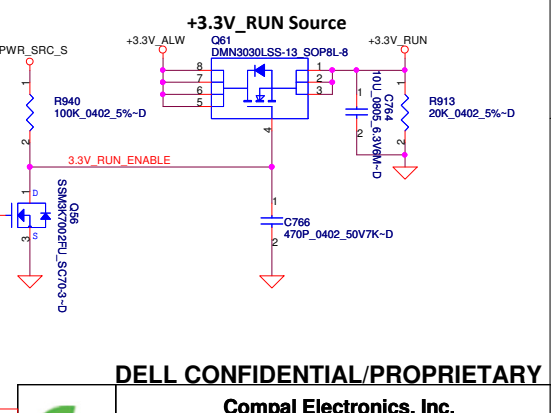
+3.3V_SUS Source

The schematic shows the internal circuitry of the +3.3V_SUS pin. It is a MOSFET-based voltage source. The gate of MOSFET Q53A is driven by the SUS_ON signal (3.3V#) through a 100K resistor R915. The drain of Q53A is connected to the +3.3V_SUS output. The source of Q53A is connected to ground. A MOSFET Q54 is also present, with its gate connected to the SUS_ENABLE signal through a 100K resistor R911. The drain of Q54 is connected to the +3.3V_SUS output. The source of Q54 is connected to ground. The output +3.3V_SUS is filtered by a 10uF capacitor C765 and a 20K resistor R914. A 4700pF capacitor C767 is connected to the output. A 1M resistor R1818 is connected to the SUS_ENABLE signal.


[illegible][illegible]


+3.3V_RUN Source


The schematic diagram illustrates the +3.3V_RUN Source circuit. It features a MOSFET (Q58, SSM6K7002FL-SC70-3-D) controlled by the 3.3V_RUN_ENABLE signal. The MOSFET's source is connected to ground, and its drain is connected to the +3.3V_RUN output. A diode (D61, DMN3030LSS-13_SOP8L-8) is connected between the +3.3V_RUN output and the +3.3V_ALW input. A resistor (R940, 100K_0402_5%-D) is connected between the +3.3V_ALW input and the MOSFET's gate. A capacitor (C766, 470P_0402_50V7K-D) is connected between the +3.3V_RUN output and ground. A diode (C764, 10U_0805_6.3VWV-D) is connected between the +3.3V_RUN output and the +3.3V_ALW input.





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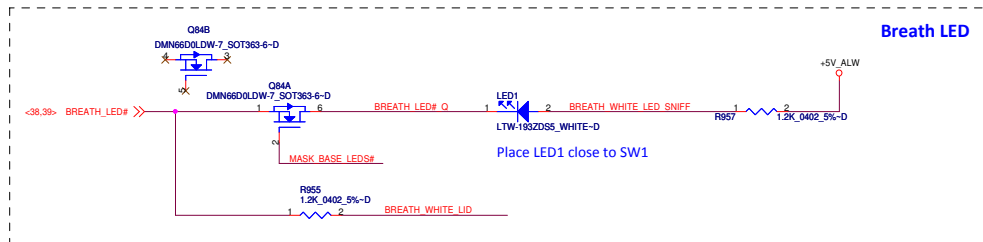
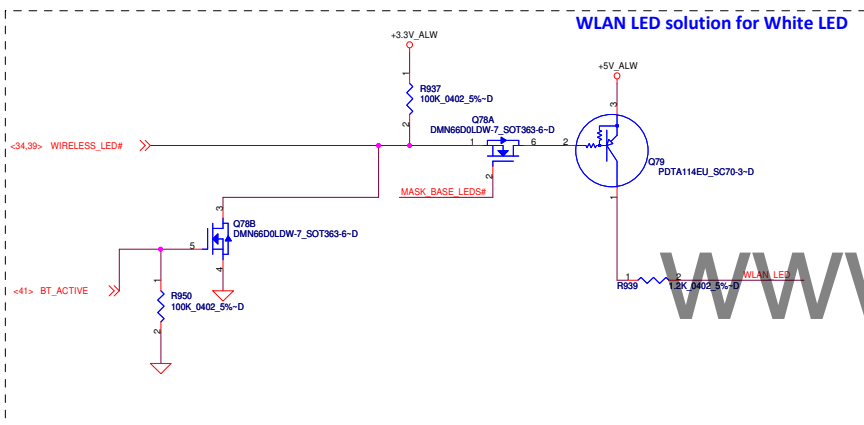
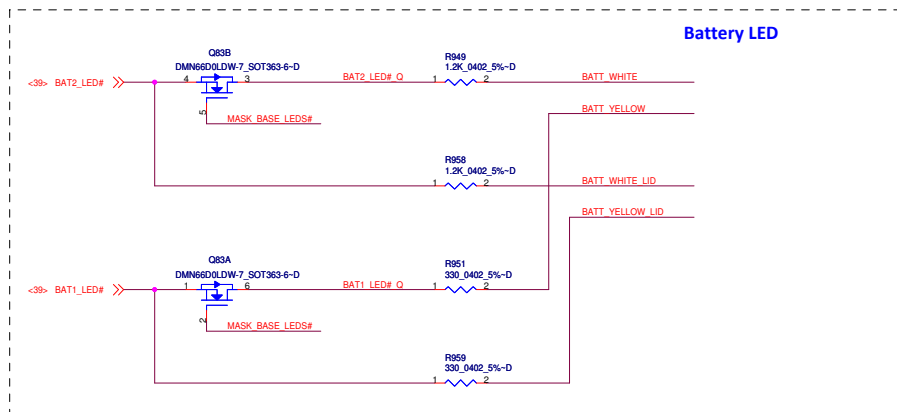
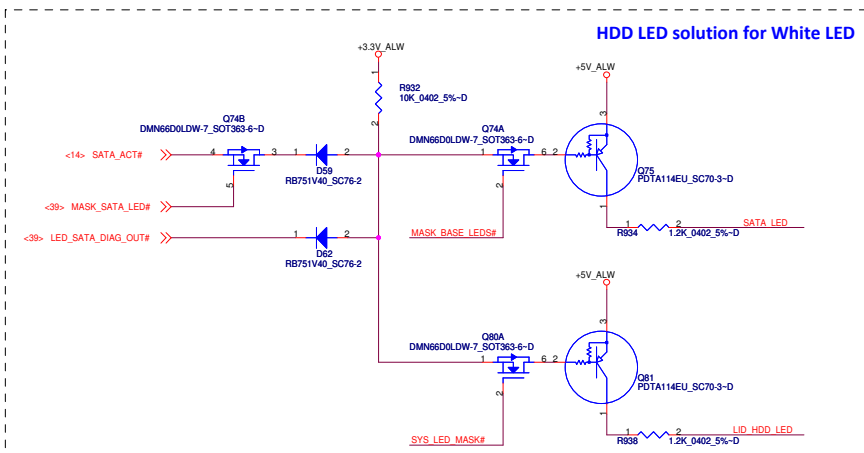
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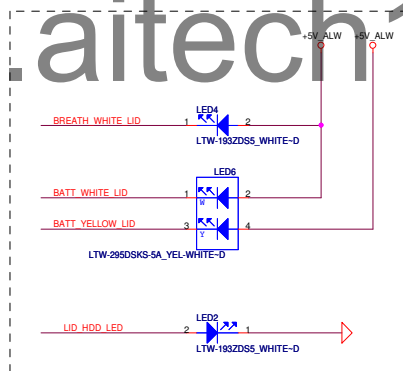
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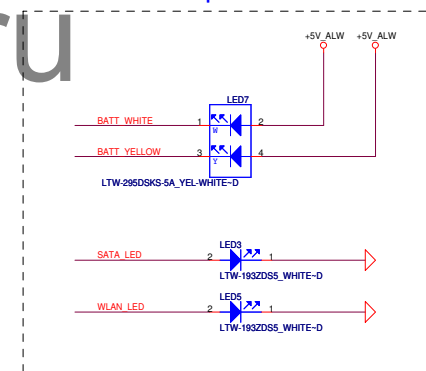
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Status LED when LID Close



Status LED when LID Open

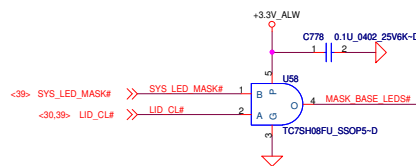
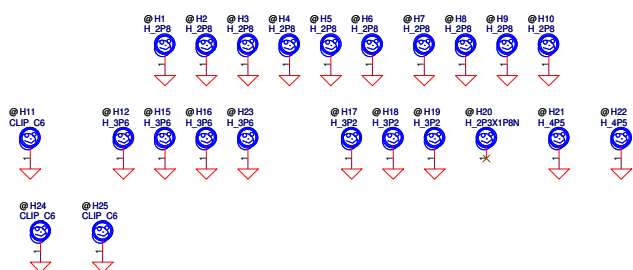


LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark

- FD1
- FIDUCIAL MARK-D
- FD2
- FIDUCIAL MARK-D
- FD3
- FIDUCIAL MARK-D
- FD4
- FIDUCIAL MARK-D



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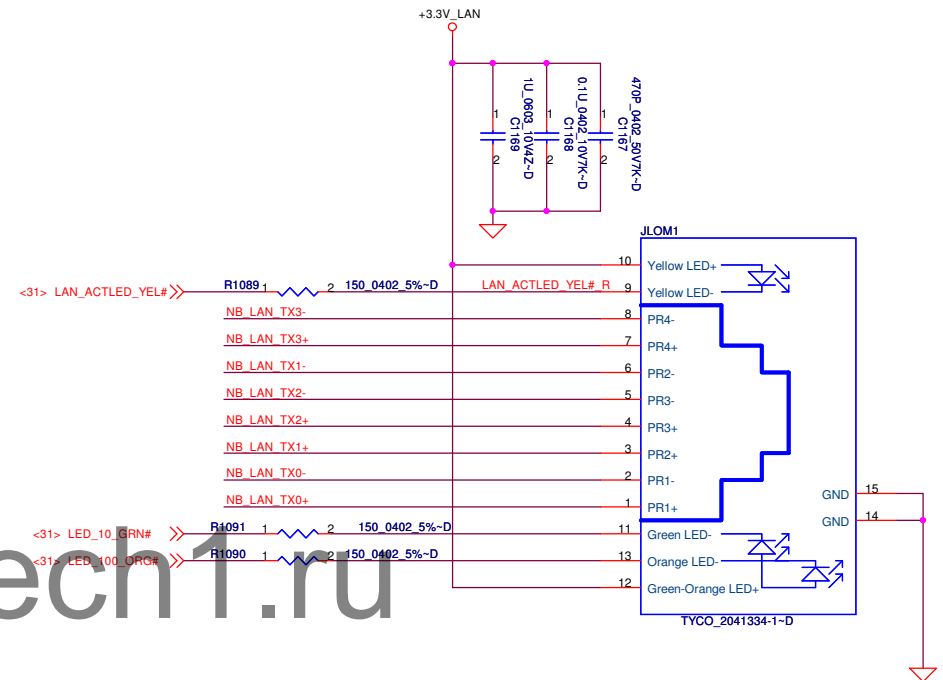
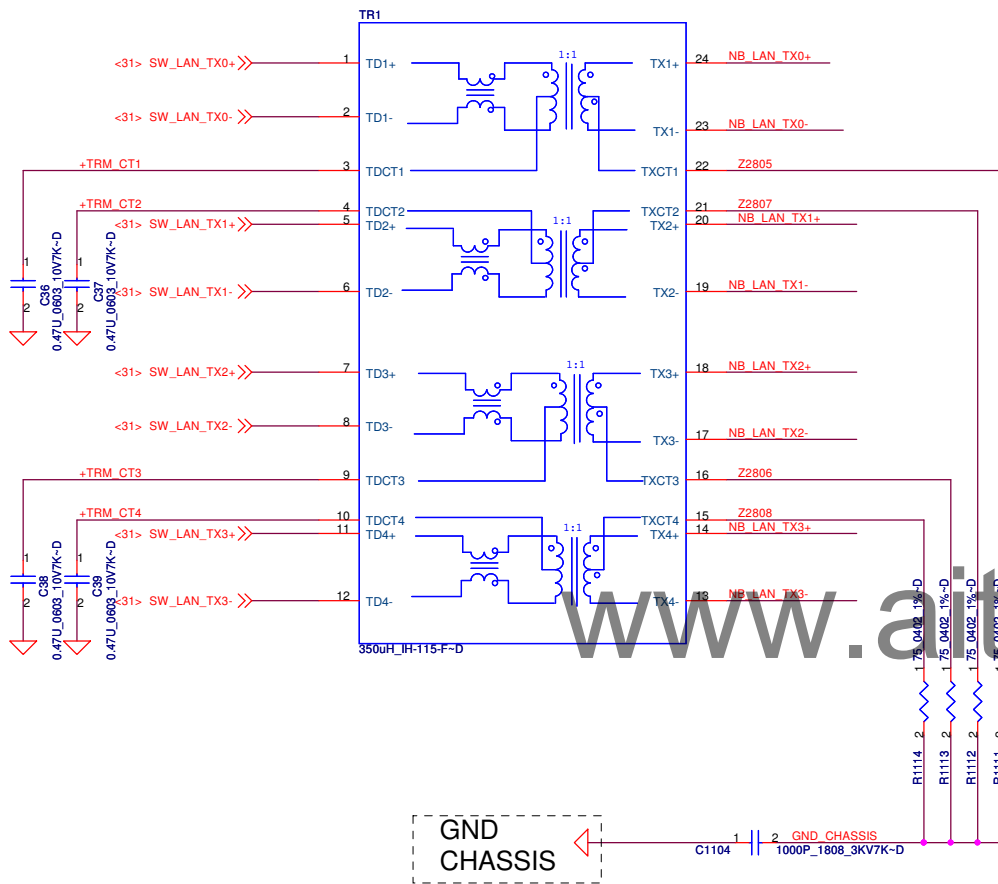
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PAD and Standoff

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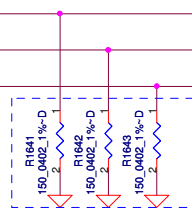
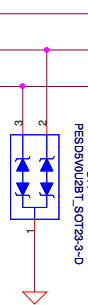
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<23> BLUE_CRT

ESD ask to add D77, D83

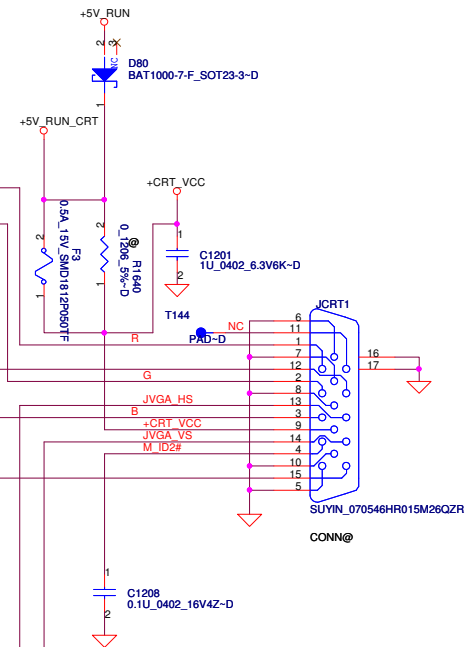
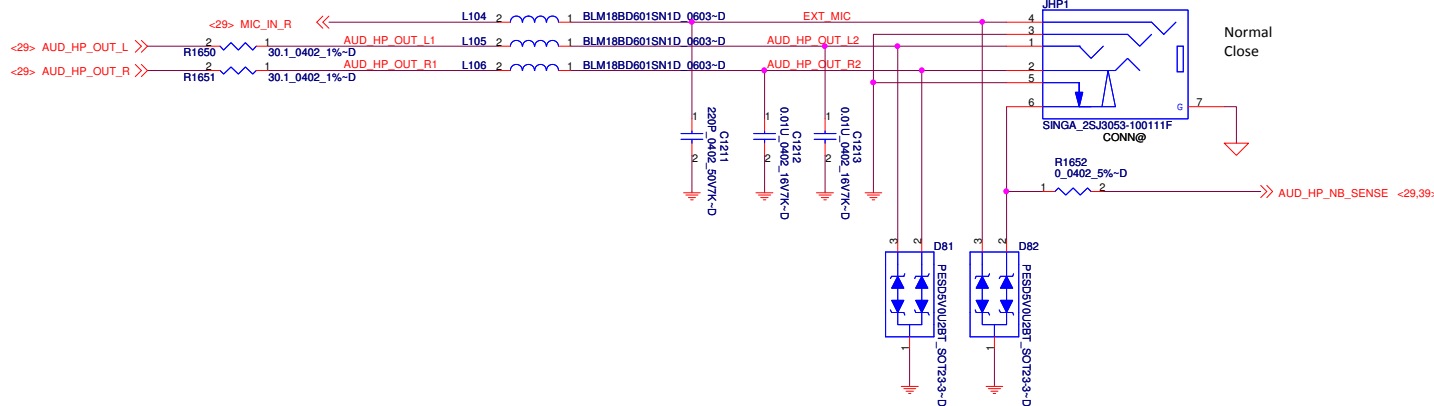


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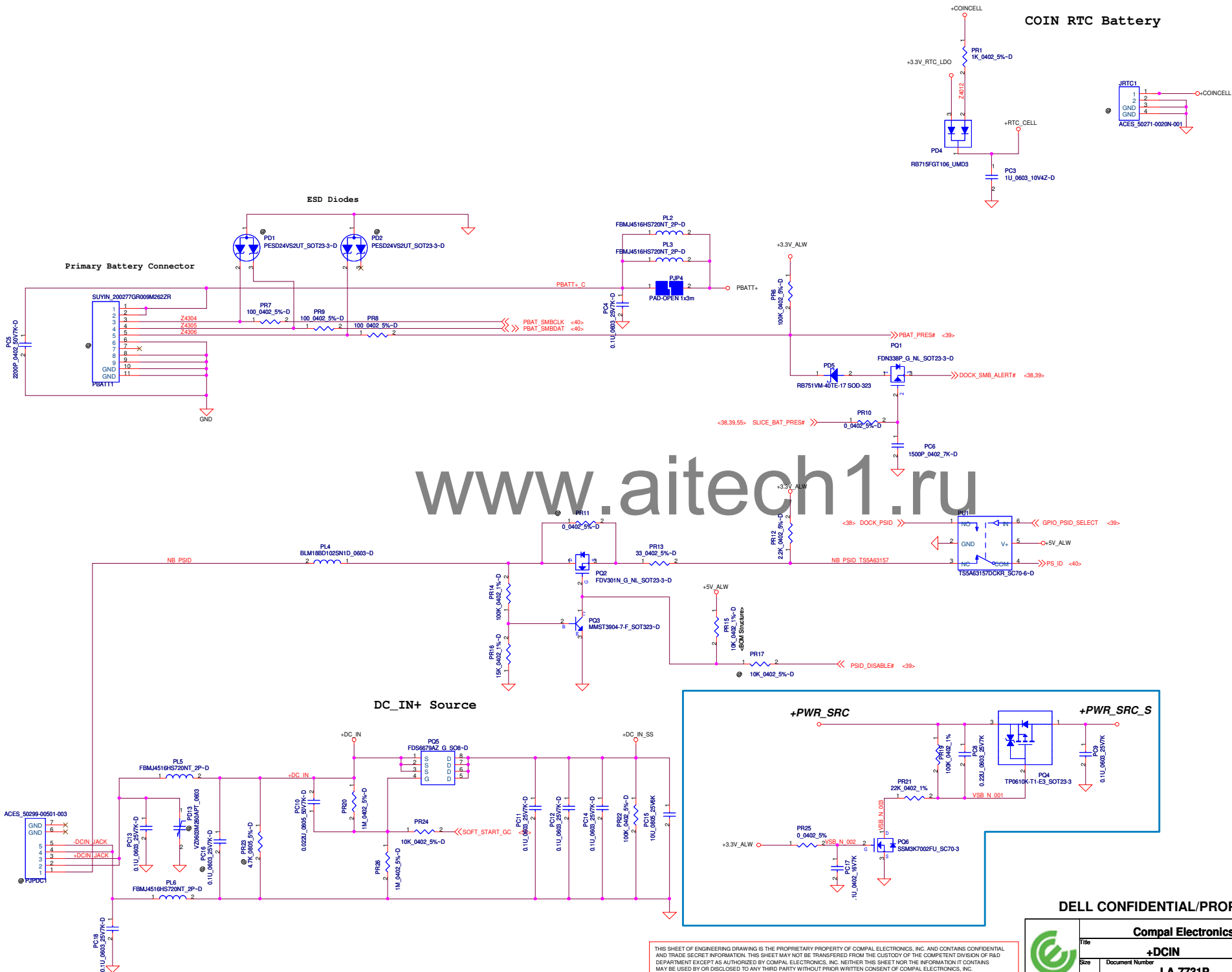
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Combo Jack



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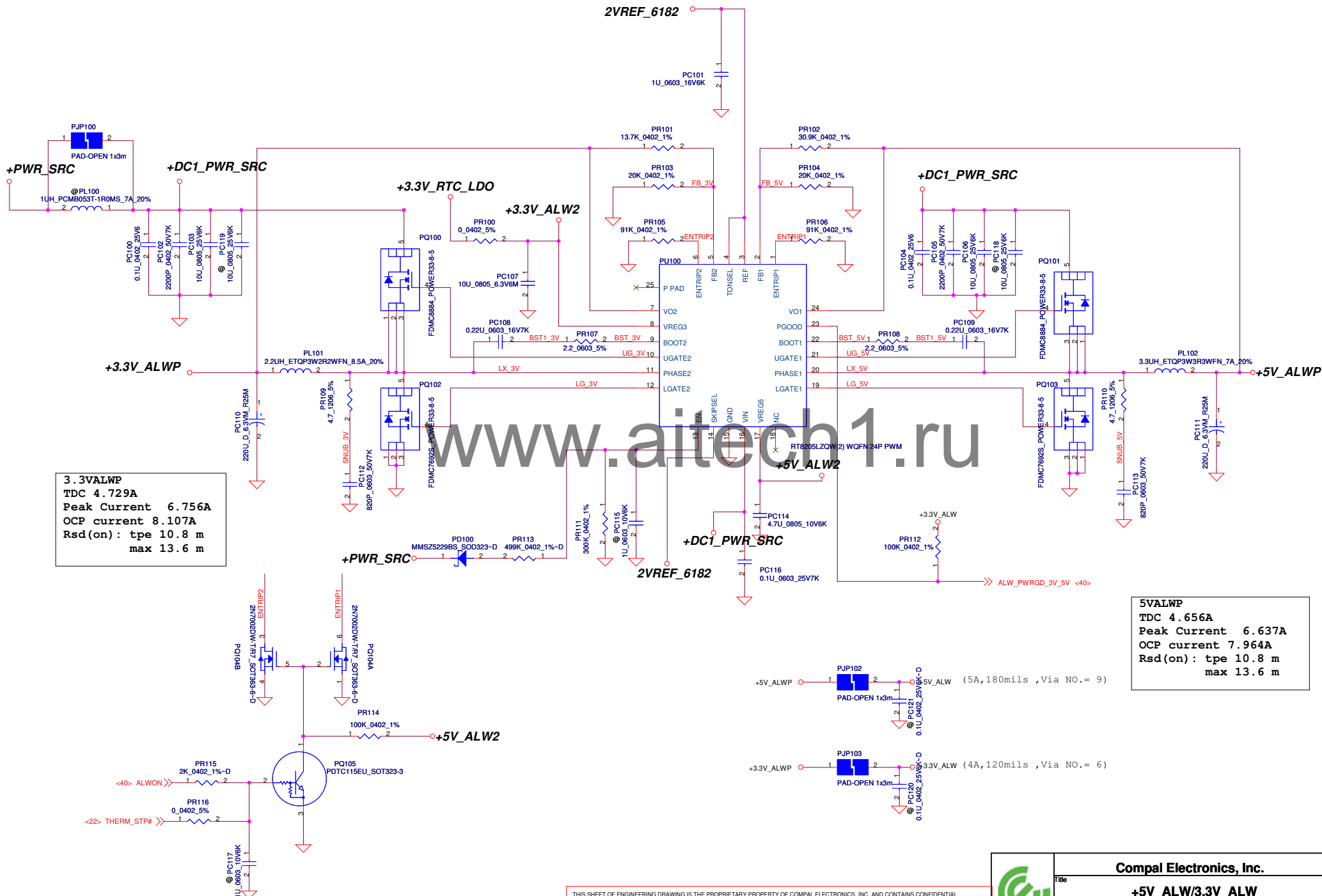
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CRT & Combo Jack			
LA-7731P			
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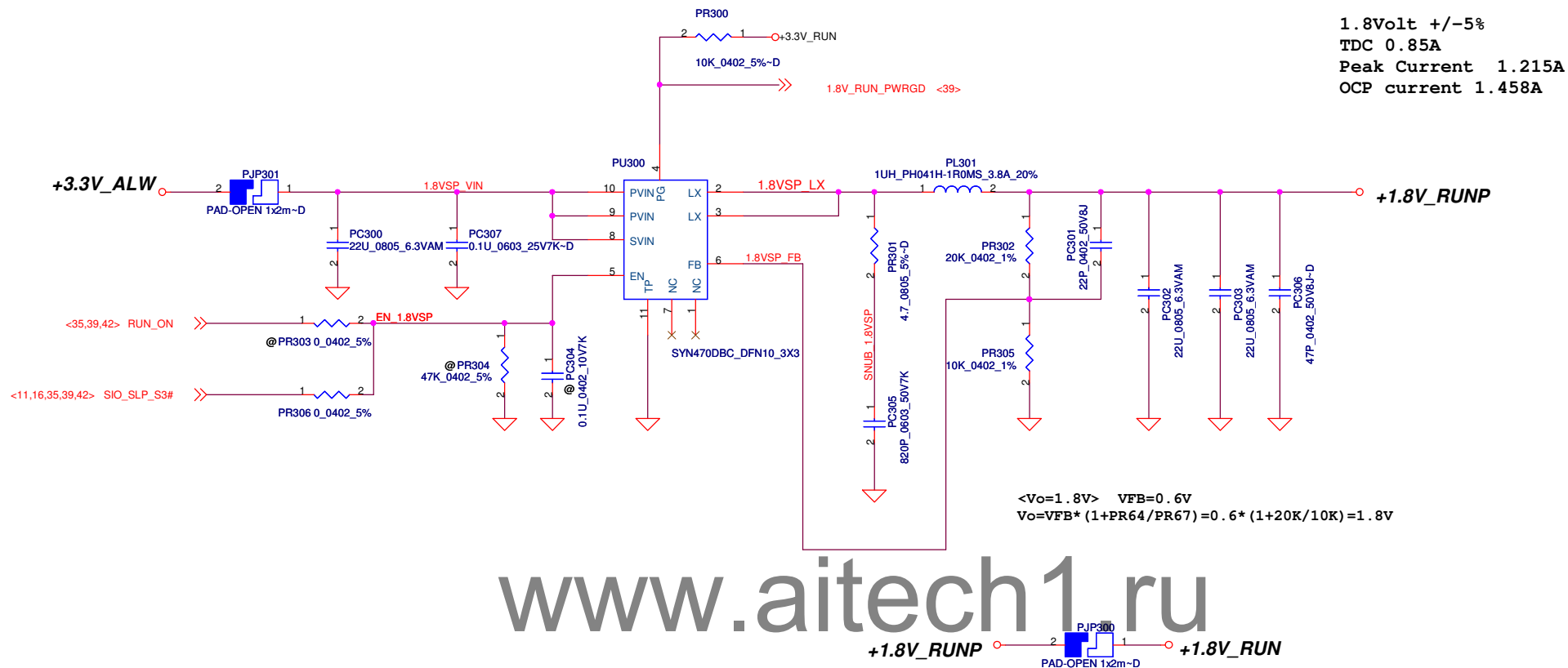
3.3VALWP
TDC 4.729A
Peak Current 6.756A
OCP current 8.107A
Rsd(on): tpe 10.8 m
max 13.6 m

5VALWP
TDC 4.656A
Peak Current 6.637A
OCP current 7.964A
Rsd(on): tpe 10.8 m
max 13.6 m

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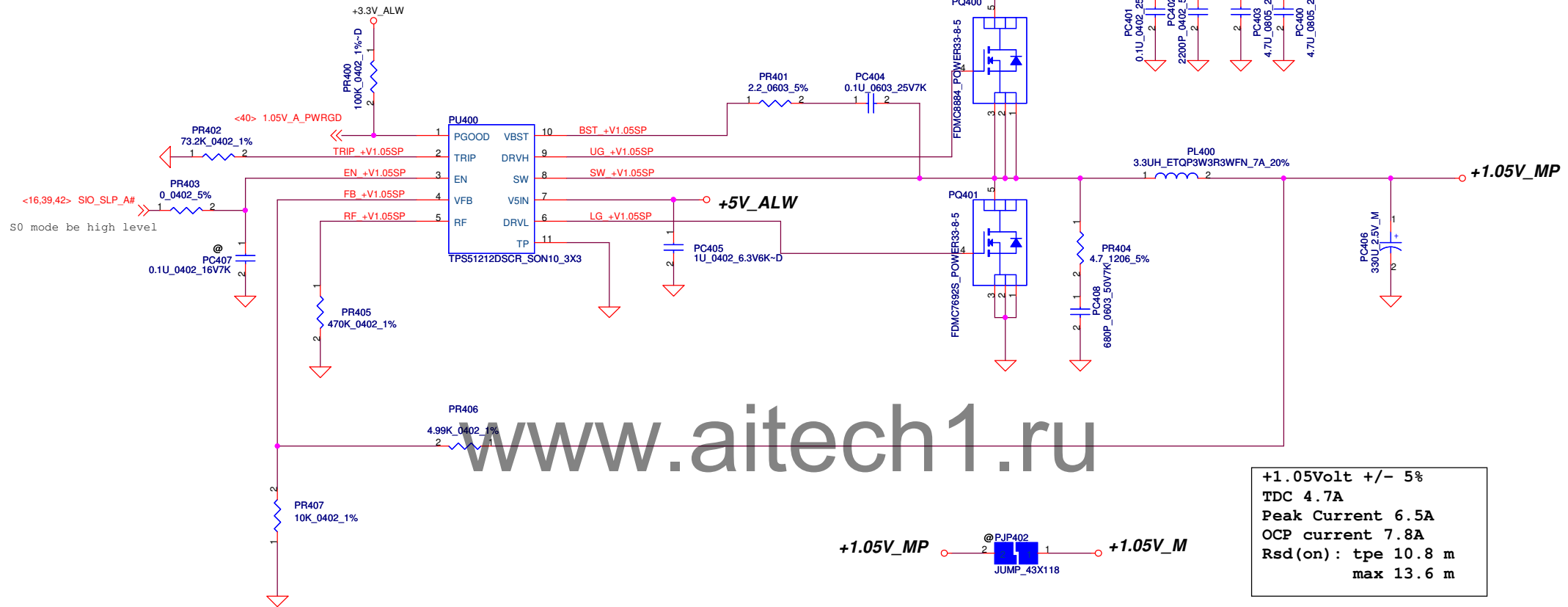
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Title			
+5V_ALW/3.3V_ALW			
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Title			
+1.8V_RUN			
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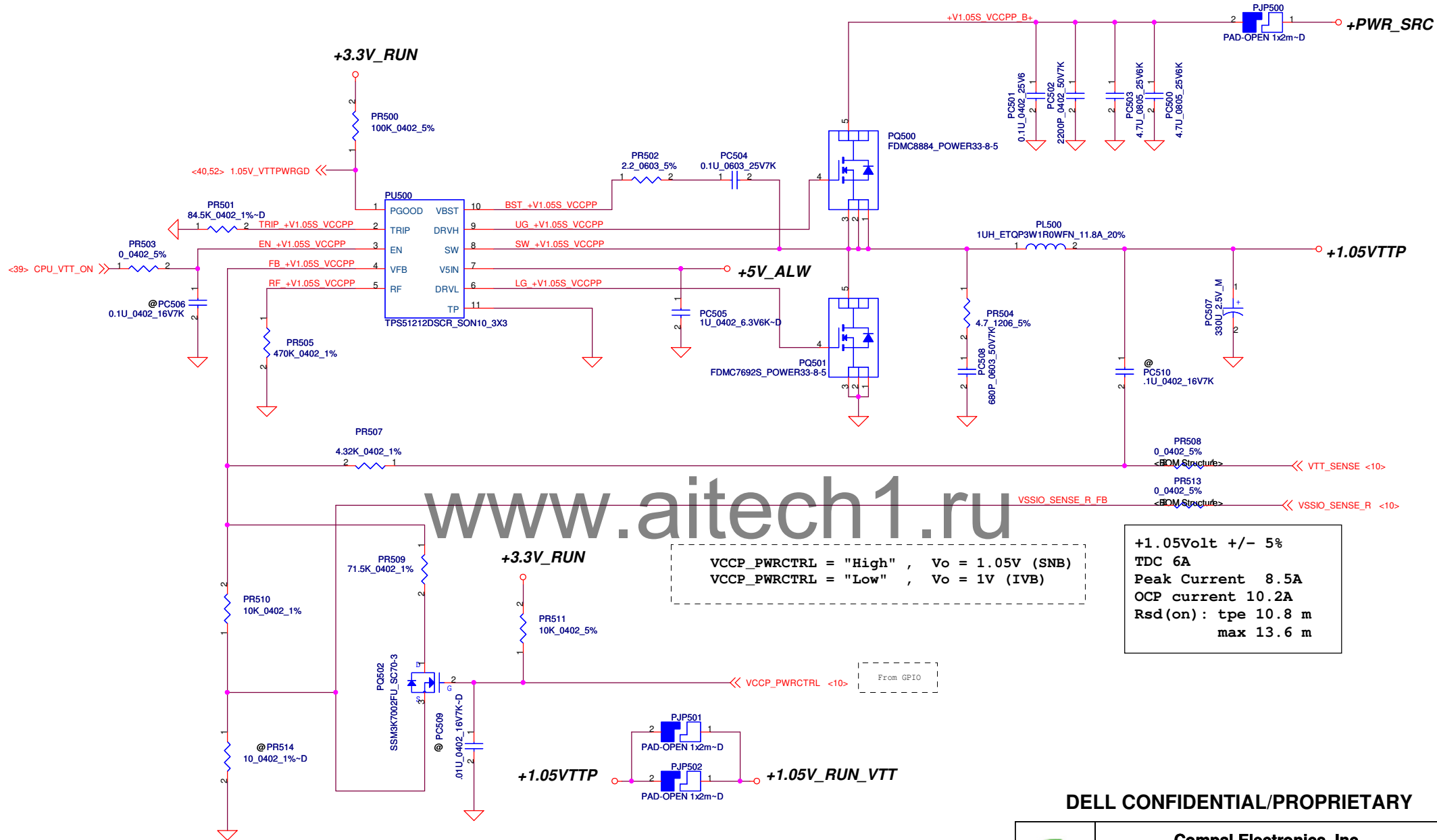
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+1.05V_M		
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+1.05V_RUN_VTT		
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+3.3V_ALW

GND_VCCSA

+5V_ALW

+3.3V_RUN

The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

VCCSA
TDC 4.2A
Peak Current 6A
OCP current 7.2A

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+VCCSA_P

GND_VCCSA

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+VCC SA

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Rev	0.3
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ISL88731C

E2 AC_OK=17.7 Volt

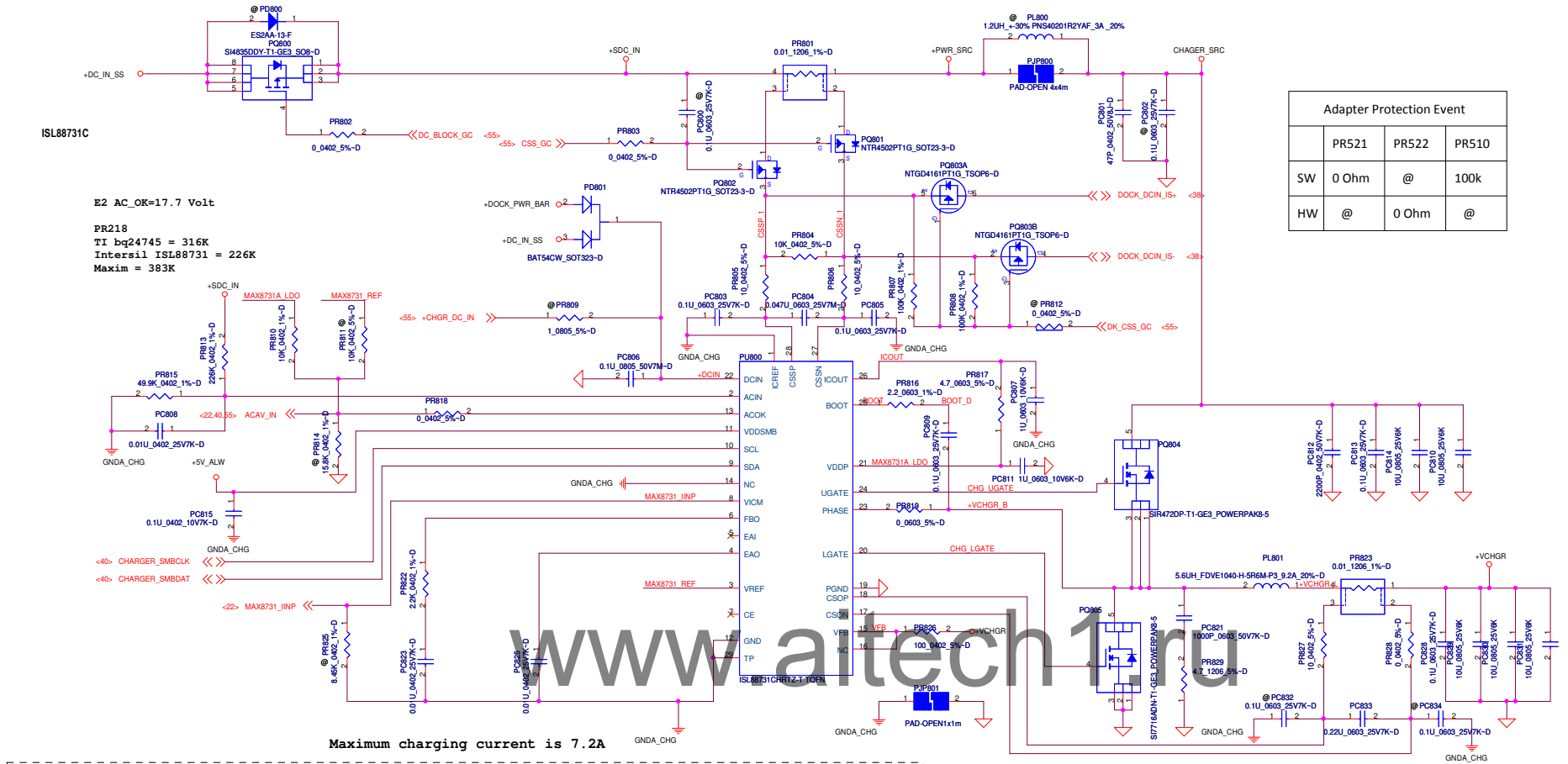
PR218

TI bq24745 = 316K

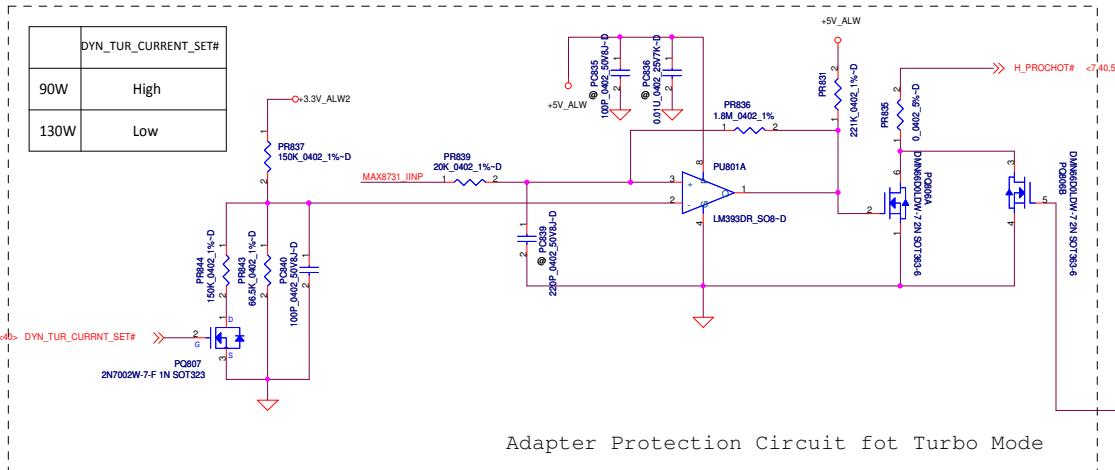
Intersil ISL88731 = 226K

Maxim = 383K

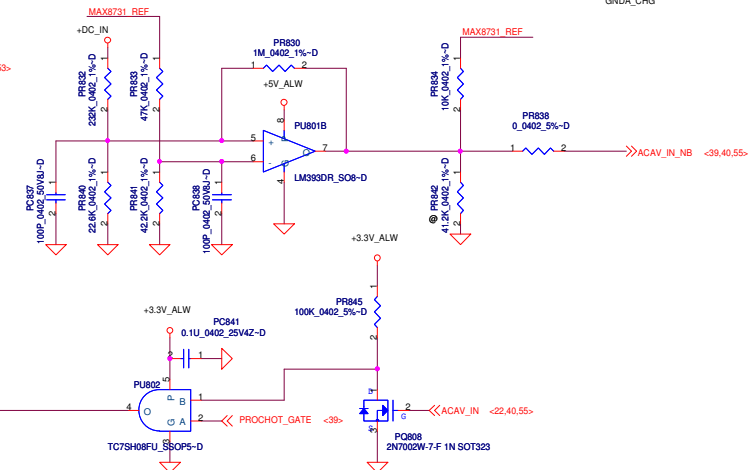
Adapter Protection Event			
	PR521	PR522	PR510
SW	0 Ohm	@	100k
HW	@	0 Ohm	@



Maximum charging current is 7.2A



Adapter Protection Circuit for Turbo Mode

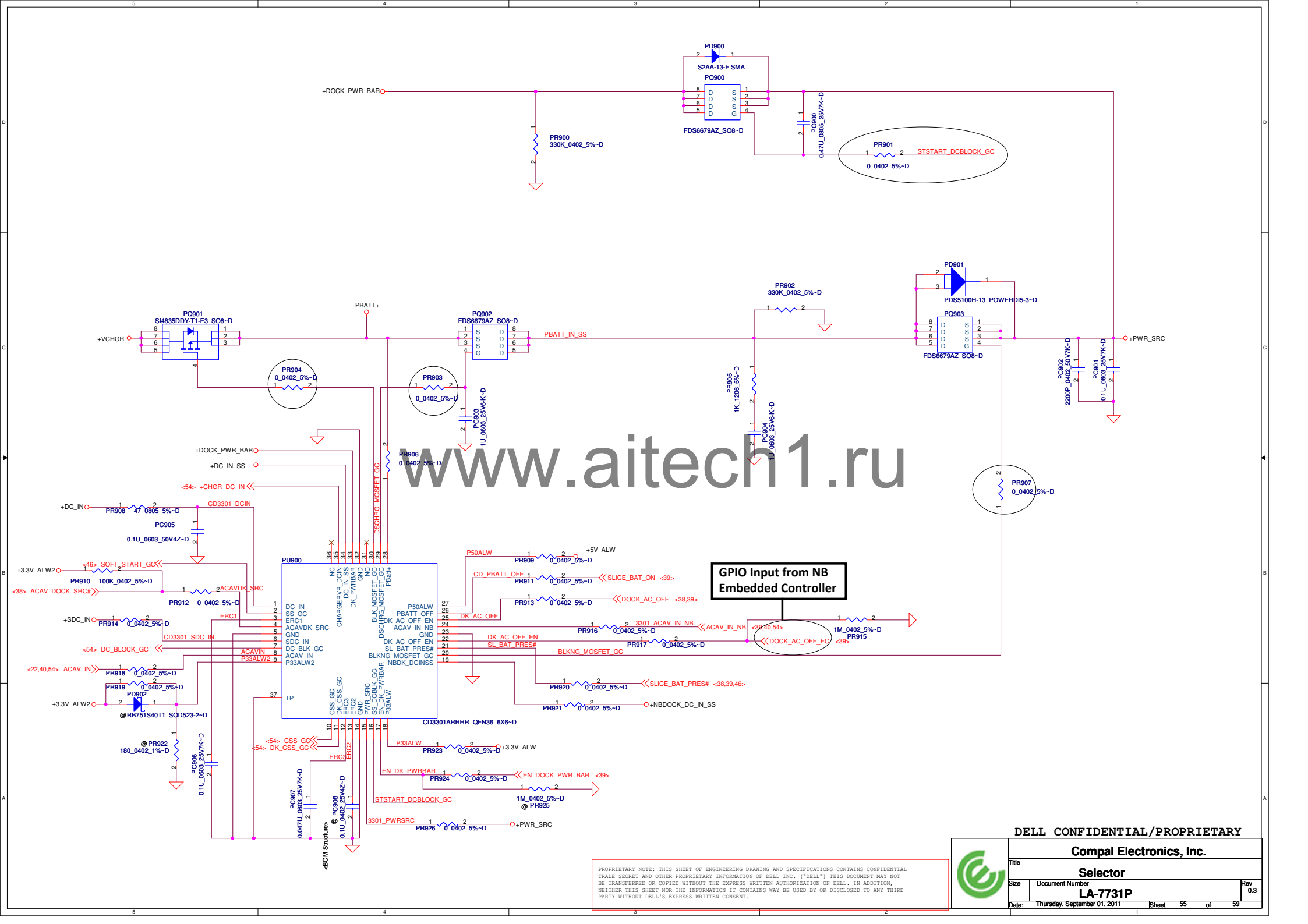


To preset system to throttle switching from AC to DC


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Charger			
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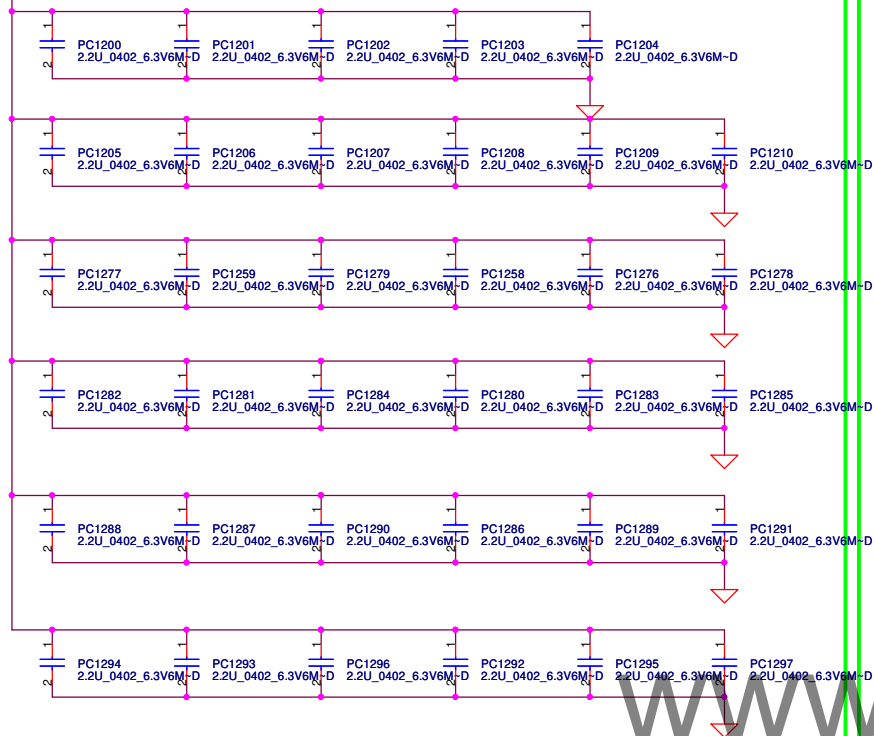
Compal Electronics, Inc.

Selector

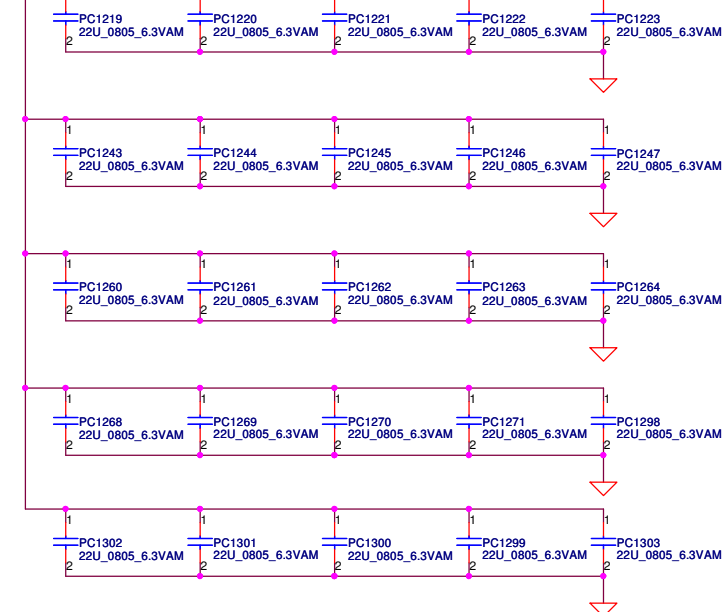
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+VCC_CORE



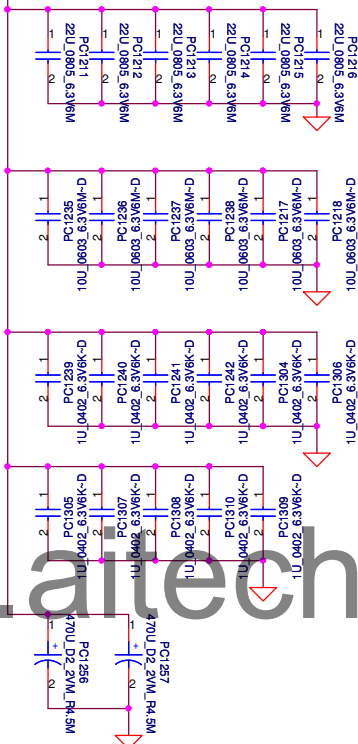
+VCC_CORE



+VCC_CORE

+VCC_GFXCORE

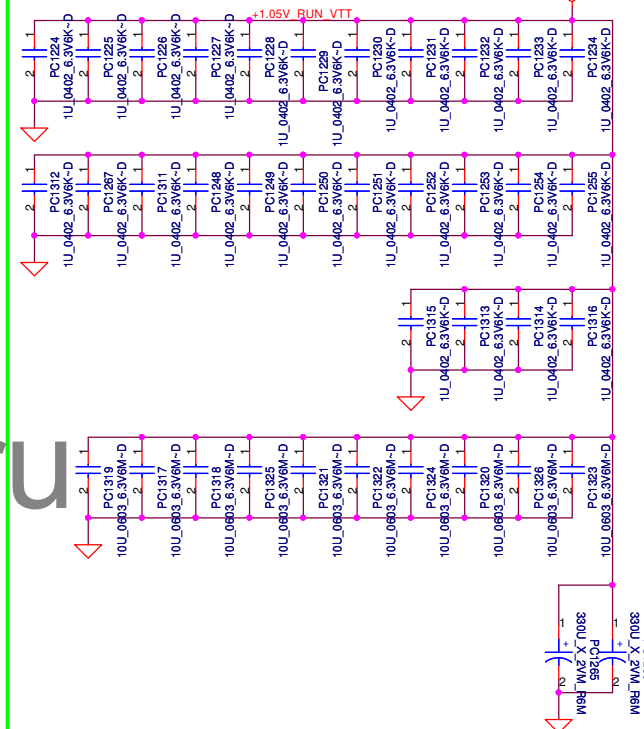
+VCC_GFXCORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

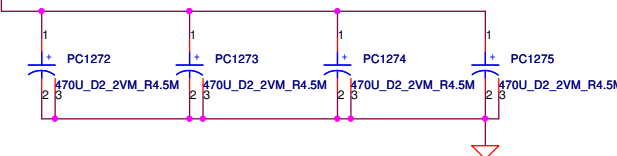
Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+1.05V_RUN_VTT



+VCC_CORE

+VCC_CORE



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PROCESSOR DECOUPLING


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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	48	+1.5V_MEN	8/16	Dell	Follow VC , enable use SIO_SLP_S4#.	Add PR210 for net "SIO_SLP_S4#"	X01
2	46	DCIN	8/16	Dell	ME design change.	PJPDC1 change from 7pin to 5pin	X01
3	47	+5V/3.3V	8/16	Dell	Main and 2nd IC common setting.	De-pop PD100,PR113,PR111	X01
4	53	Vcore/GFX core	8/16	Compal RF_team	Suppress WWAN BB noise.	Pop PC751,PR760,PC725,PR731, PC745,PR751(680pF 0603, 4.7 ohm 1206)	X01
5	50 51	+1.05VM/ +1.05VTT	8/16	Compal	COS concern, change from D2 Polymer cap to OScon cap	PC406, PC507	X01
6	53	Vcore/GFX core	8/16	Compal	Prevent output voltage glitch when power up.	PU700 VCCP and VDD change form +5V_RUN to +5V_ALW	X01
7	47,53 ,54	Vcore, Charger +5V/3.3V	8/16	Compal RF_team	EMI solution.	Pop PL700.PL1300,PL100	X01
8	53	Vcore/GFX core	8/16	Compal	adjust OCP and DC load line.	PR740 change to 2.1k ohm, PR750 change to 392 ohm.	X01
9							X01
10							X01
11							X01
12							X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	39, 40, 42	HW	7/14/2011	DELL	E4 uses SIO_SLP_S4# for power control	Add @R752, R753	X01
2	11	HW	7/14/2011	Compal	Change DDR channel A signal to DSL	Add CC149, CC152, CC178, CC179	X01
3	18	HW	7/26/2011	DELL	Follow GPIO map rev1.0	Change RH273 from 1k to 10k	X01
4	29	HW	7/26/2011	Compal	EMI request	Pop CE981, CE982, CE983	X01
5	35	HW	7/26/2011	Compal	Solve Express card PAID issue	Add R830	X01
6	7, 22	HW	7/27/2011	Compal	Solve ESD issue	Reserve D84, D85	X01
7	25	HW	7/27/2011	Compal	Layout routing	Swap HDMI trace connection on L19, L20, L21, L22 for layout routing	X01
8	29	HW	7/28/2011	Compal	EMI request	Add CE984, CE985	X01
9	7	HW	8/1/2011	Compal	EMI request	Reserve CC141	X01
10	17	HW	8/3/2011	Intel	Request from Intel review feedback	Pop RH332	X01
11	14, 39	HW	8/4/2011	SMSC	SMSC request to delete LPC_LDRQ0#	Leave LDRQ0# no connection on both of 5048 and PCH side	X01
12	20, 42	HW	8/4/2011	Compal	Vgs less than cut-in voltage in battery mode	Add QH6, RH279, CH107	X01
13	42	HW	8/4/2011	Compal	Load SW sources output rising time mismatch and COS. cost concern.	Change back to E3 +3.3V/5V RUN discrete solution. Add Q55, Q56, Q61, Q62, R933, R940, R1627, remove U78, R749, R747, C1199, C1198, C1197, C1196, change C761, C764 to 10uF	X01
14	10	HW	8/4/2011	Compal	Follow INTEL PDDG 0.8	De-pop RC140	X01
15	32	HW	8/4/2011	Compal	RESET_OUT# power sequence issue	Add R1653, 1M ohms pull down for USH_PWR_STATE# at M/B side	X01
16	40	HW	8/4/2011	COMPAL	Change board ID to X01	Change R875 to 130Kohms	X01
17	34	HW	8/4/2011	COMPAL	PCH GPIO52 need 8.2~10K pull up +3.3VS	Change R695 from 100K to 10Kohms	X01
18	23	HW	8/4/2011	COMPAL	CRT SW 2nd source TI, TS3V713 pin29 is VDD	Connect pin29 to +3.3V_RUN	X01
19	16	HW	8/4/2011	COMPAL	+1.05V_M turn off before APWROK de-assert	Add UH5 circuit for backup HW solution	X01
20	41	HW	8/4/2011	COMPAL	Reset IC threshold voltage issue	Change U4 to RT9801A (threshold adjustable)	X01
21	29	HW	8/4/2011	COMPAL	Co-lay 92HD93 with ALC290	Pop option for 92HD93/ALC290=>R1646/C1164; R1644/R1643; C965/R1642 Reserve for ALC290 only: C1204, C1205, R171, R1647, C1165, R1648 Reserve for 92HD93 only: R1645, C963	X01
22	29	HW	8/4/2011	COMPAL	Codec is change to 92HD93	Pop R162~R166 and de-pop U73	X01
23	40	HW	8/8/2011	COMPAL	Please depop VOL MUTE/UP/DOWN due to EC code enable internal PU resistors (3V_ALW)	De-pop R1169, R1197, R1118	X01
24	41	HW	8/8/2011	COMPAL	For debug purpose	Add R1624	X01
25	42	HW	8/8/2011	COMPAL	power suggestion	Change Q59 to A04728L	X01
26	43	HW	8/9/2011	COMPAL	Align with E4	Change LED6, LED7 power source from +3.3V_ALW to +5V_ALW	X01
27	14, 40	HW	8/10/2011	COMPAL	Crystal EA result	Change C741, C743 from 22p to 39p, CH2, CH3 from 15p to 18p, CH18, CH19 from 12p to 10p for crystal EA	X01
28	41	HW	08/11/2011	COMPAL	For RSMRST# debug	Reserve R1655 and pop R1623	X01
29	26	HW	08/11/2011	COMPAL	DPX_CA_DET voltage too low through dongle	Change U21 and U24 to SA000055G0L	X01
30	43	HW	08/11/2011	COMPAL	Tune white light LED brightness	Change R934, R938, R939, R949, R958, R957 and R955 to 2.2K ohm	X01

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31	20, 22, 34 38, 39, 43	HW	8/11/2011	COMPAL	Cost saving	Change D2, D31, D32, D34, D59, D62, DH2, DH3, D65, D66, D67, D68, D69, D70 to SCS00002G00	X01
32	11	HW	8/12/2011	COMPAL	Solve S3 wake up issue	Pop RC79 and de-pop RC82	X01
33	36, 41	HW	8/14/2011	ME	ME change connector	Change JUSB1, JUSB2, JBT1	X01
34	30	HW	8/16/2011	ME	ME change connector	Change JLID1	X01
35	17, 32 39, 40	HW	8/18/2011	COMPAL	RF request	Pop R885, C747, R795, C713, RE5 and change CE3 to 12pF and pop it, and add CH109, CH110	X01
36	36	HW	8/19/2011	COMPAL	Follow Intel design guide	Change C410~C413 from 0.01uF to 0.1uF	X01
37	25	HW	8/24/2011	COMPAL	EMI request to solve HDMI issue	Add C1216~C1223	X01
38	7	HW	8/25/2011	COMPAL	ESD request	Change RC25 to 1k and pop CC141	X01
39	40	HW	8/26/2011	SMSC	SMSC request	Reserve R941, R942	X01
40	24, 33	HW	8/26/2011	EMI	EMI request to solve SD/DMIC issue	Reserve CE758, CE279, CE280	X01
41	43	HW	8/27/2011	ME	Solve standoff shift issue	Change H11, H24, H25 to 6mm	X01
42	43	HW	8/29/2011	COMPAL	Tune white light LED brightness	Change R934, R938, R939, R949, R958, R957 and R955 to 1.2K ohm	X01
42	14	HW	8/29/2011	ME	change TAA connector	Change JTAA1	X01

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EE P.I.R (2/2)			
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